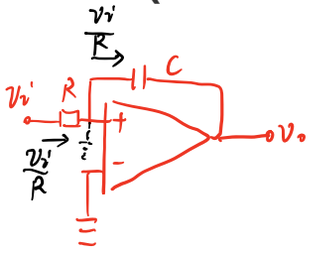
Latches, Flip-Flops, and Timers

7–1 Latches

The S-R (SET-RESET) Latch

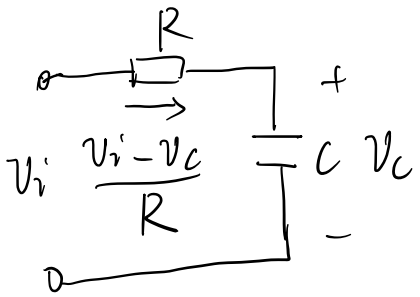


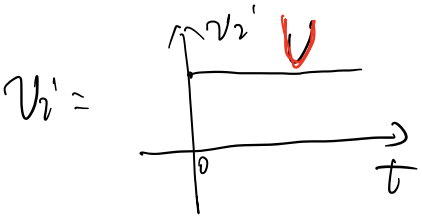
$$v_o = \frac{1}{C}\int \frac{v_i}{R}\,dt$$

$$= \frac{1}{RC}\int v_i\,dt$$

$$C = \frac{q}{v}$$

$$\Rightarrow v = \frac{1}{C}q = \frac{1}{C}\int i\,dt$$





$$\Rightarrow v_C = \frac{1}{C}\int \frac{v_i - v_C}{R}\,dt$$

$$= \frac{1}{RC}\int (v_i - v_C)\,dt$$

$$= \frac{1}{RC}\int v_i\,dt - \frac{1}{RC}\int v_C\,dt$$

$$u_C(t) = u_C(\infty) + [u_C(0^+) - u_C(\infty)]\,e^{-\frac{1}{\tau}t}$$

$$u_C(t) = u_C(\infty) + [u_C(0^+) - u_C(\infty)]\,e^{-\frac{t}{\tau}}$$

① ② ③ $\tau = RC$

① $u_C(\infty) = V$

② $u_C(0^+) = 0\,V$

$$= V - Ve^{-\frac{t}{RC}} \quad (t \geq 0)$$

R	S	Q^n	Q^{n+1}	$\overline{Q^{n+1}}$	
0	0	Q^n	Q^n	$\overline{Q^n}$	← 保持
0	1	1	0	1	← 置'1'
1	0	0	1	0	← 置'0'
1	1	0	0	1	← 不穩定

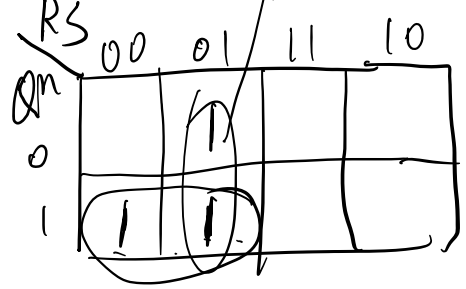
$\overline{R}$	$\overline{S}$	Q^{n+1}	$\overline{Q^{n+1}}$	
0	0	1	1	← 不穩定
0	1	0	1	← 置'0'
1	0	1	0	← 置'1'
1	1	Q^n	$\overline{Q^n}$	← 保持

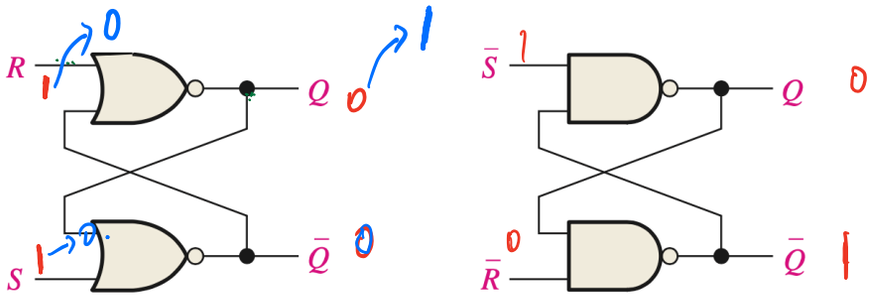
R	S	Q^n	Q^{n+1}	$\overline{Q^{n+1}}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

$RS = 0$

$$Q^{n+1} = \bar{R}\bar{S}Q^n + \bar{R}S\bar{Q}^n + \bar{R}SQ^n$$

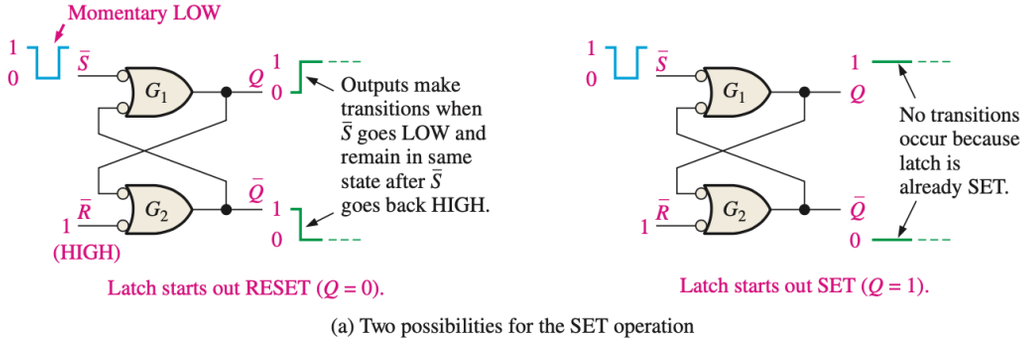
$$= \bar{R}S + \bar{R}Q^n, \qquad RS = 0$$



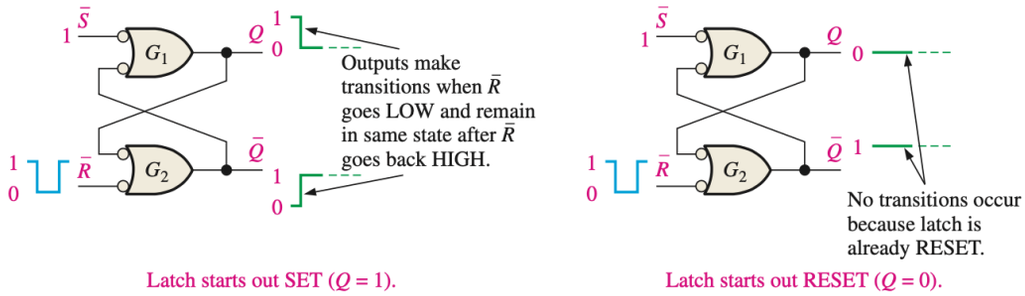


(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

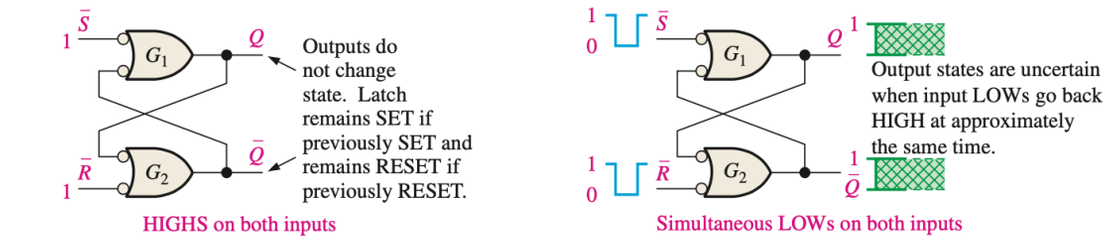
FIGURE 7–1 Two versions of SET-RESET (S-R) latches. Open files F07-01(a) and (b) and verify the operation of both latches. *A Multisim tutorial is available on the website.*



(a) Two possibilities for the SET operation



(b) Two possibilities for the RESET operation



(c) No-change condition (d) Invalid condition

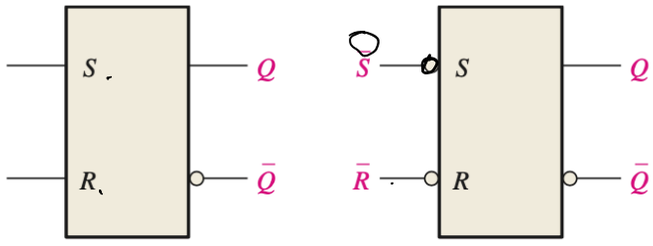
FIGURE 7–3 The three modes of basic $\overline{S}$-$\overline{R}$ latch operation (SET, RESET, no-change) and the invalid condition.

TABLE 7–1

Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Logic symbols for both the active-HIGH input and the active-LOW input latches are shown in Figure 7–4.



(a) Active-HIGH input S-R latch

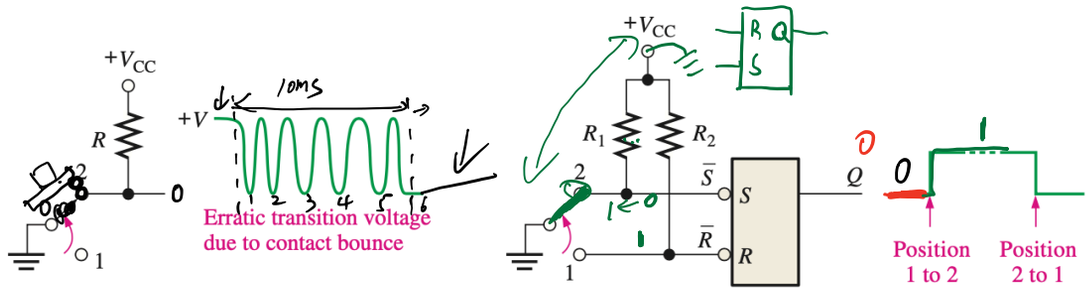
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

FIGURE 7–4 Logic symbols for the S-R and $\overline{S}$-$\overline{R}$ latch.

An Application

The Latch as a Contact-Bounce Eliminator

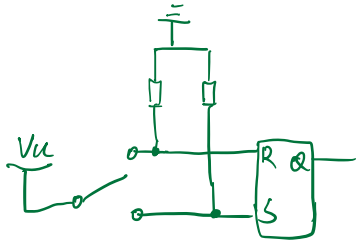
A good example of an application of an $\overline{S}$-$\overline{R}$ latch is in the elimination of mechanical switch contact "bounce." When the pole of a switch strikes the contact upon switch closure, it physically vibrates or bounces several times before finally making a solid contact. Although these bounces are very short in duration, they produce voltage spikes that are often not acceptable in a digital system. This situation is illustrated in Figure 7–6(a).



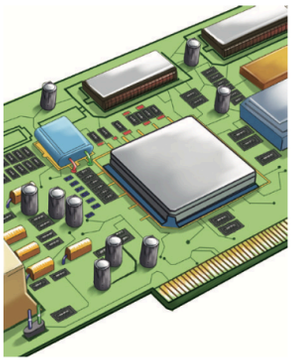
(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

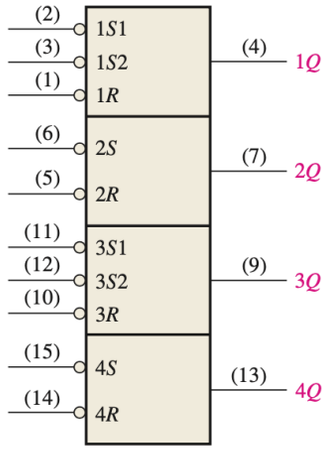
FIGURE 7–6 The $\overline{S}$-$\overline{R}$ latch used to eliminate switch contact bounce.


Vu
R
Q
S

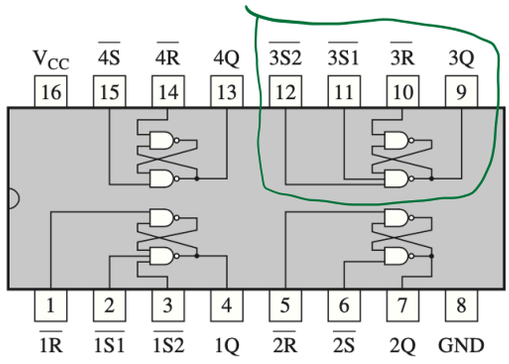
IMPLEMENTATION: $\overline{S}$-$\overline{R}$ LATCH



Fixed-Function Device The 74HC279A is a quad $\overline{S}$-$\overline{R}$ latch represented by the logic diagram of Figure 7–7(a) and the pin diagram in part (b). Notice that two of the latches each have two $\overline{S}$ inputs.



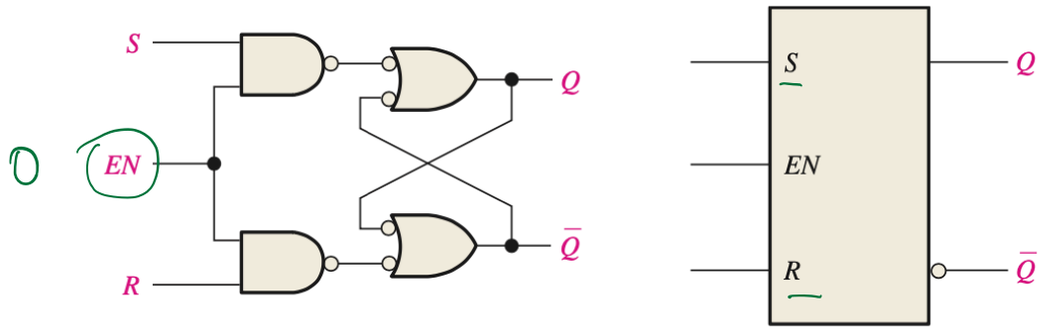
(a) Logic diagram



(b) Pin diagram

FIGURE 7–7 The 74HC279A quad $\overline{S}$-$\overline{R}$ latch.

The Gated S-R Latch



(a) Logic diagram (b) Logic symbol

FIGURE 7–8 A gated S-R latch.

EXAMPLE 7–2

Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

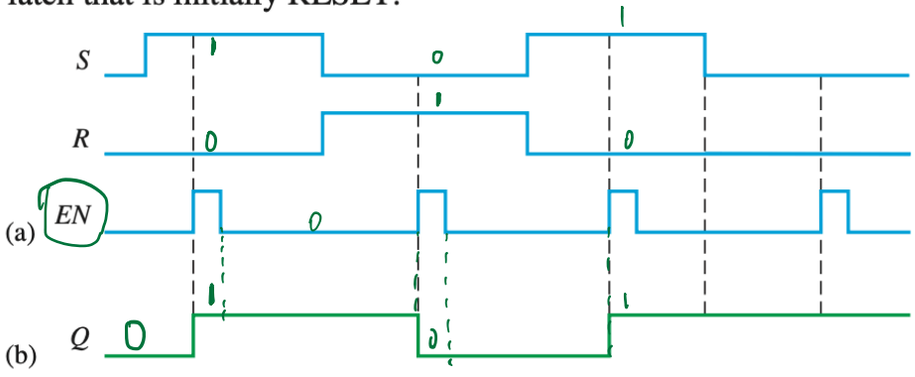
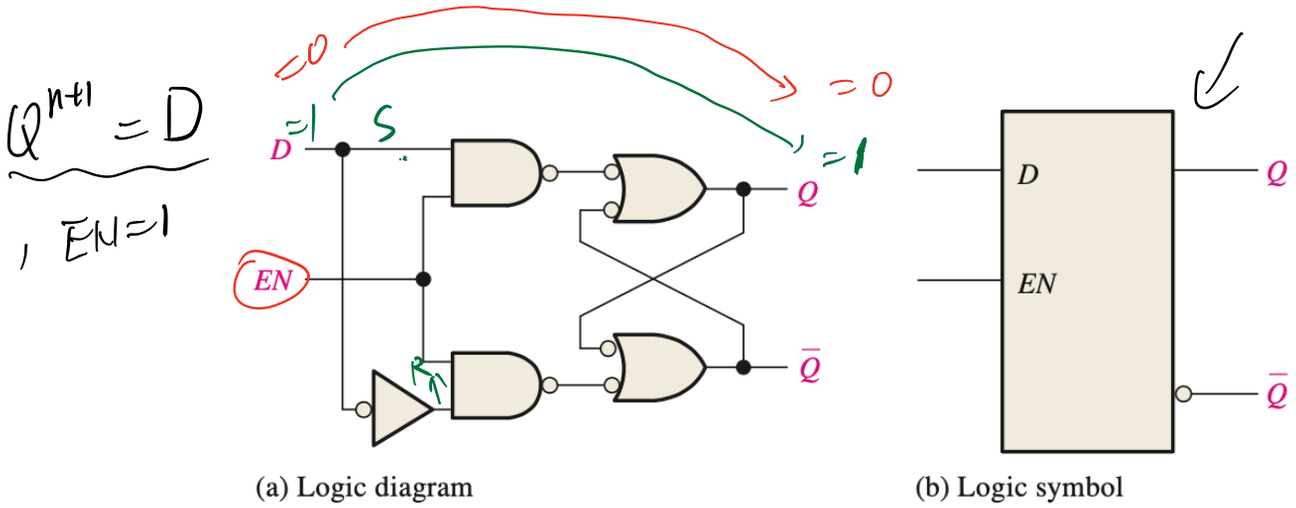


FIGURE 7–9

The Gated D Latch



(a) Logic diagram (b) Logic symbol

FIGURE 7–10 A gated D latch. Open file F07-10 and verify the operation.

EXAMPLE 7–3

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.

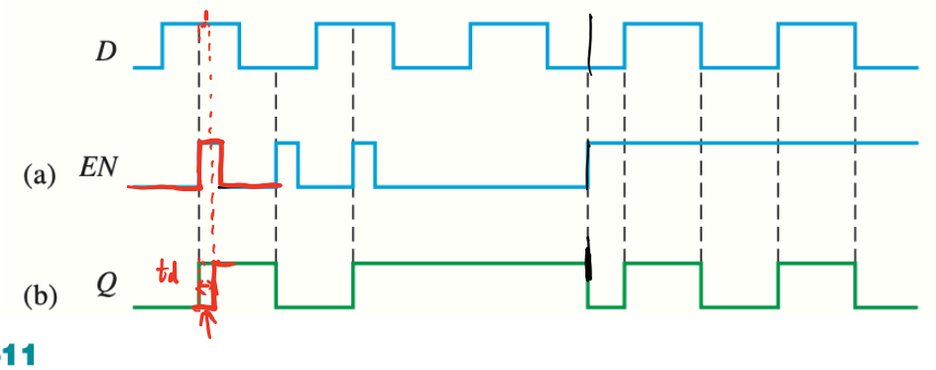
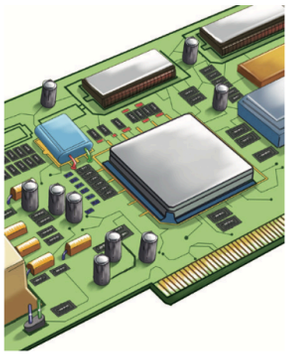
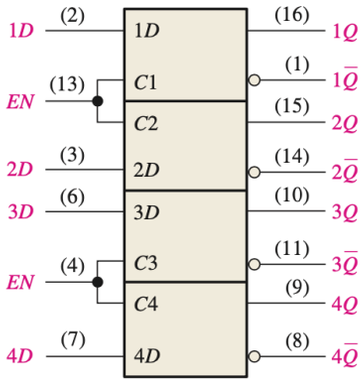


FIGURE 7–11

IMPLEMENTATION: GATED D LATCH



Fixed-Function Device An example of a gated D latch is the 74HC75 represented by the logic symbol in Figure 7–12(a). The device has four latches. Notice that each active-HIGH *EN* input is shared by two latches and is designated as a control input (*C*). The truth table for each latch is shown in Figure 7–12(b). The X in the truth table represents a "don't care" condition. In this case, when the *EN* input is LOW, it does not matter what the *D* input is because the outputs are unaffected and remain in their prior states.



(a) Logic symbol

Inputs		Outputs		
D	*EN*	Q	$\overline{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

FIGURE 7–12 The 74HC75 quad D latch.

7–2 Flip-Flops

An **edge-triggered flip-flop** changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock. Two types of edge-triggered flip-flops are covered in this section: D and J-K. The logic symbols for these flip-flops are shown in Figure 7–13. Notice that each type can be either positive edge-triggered (no bubble at *C* input) or negative edge-triggered (bubble at *C* input). The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (*C*) input. This triangle is called the *dynamic input indicator.*

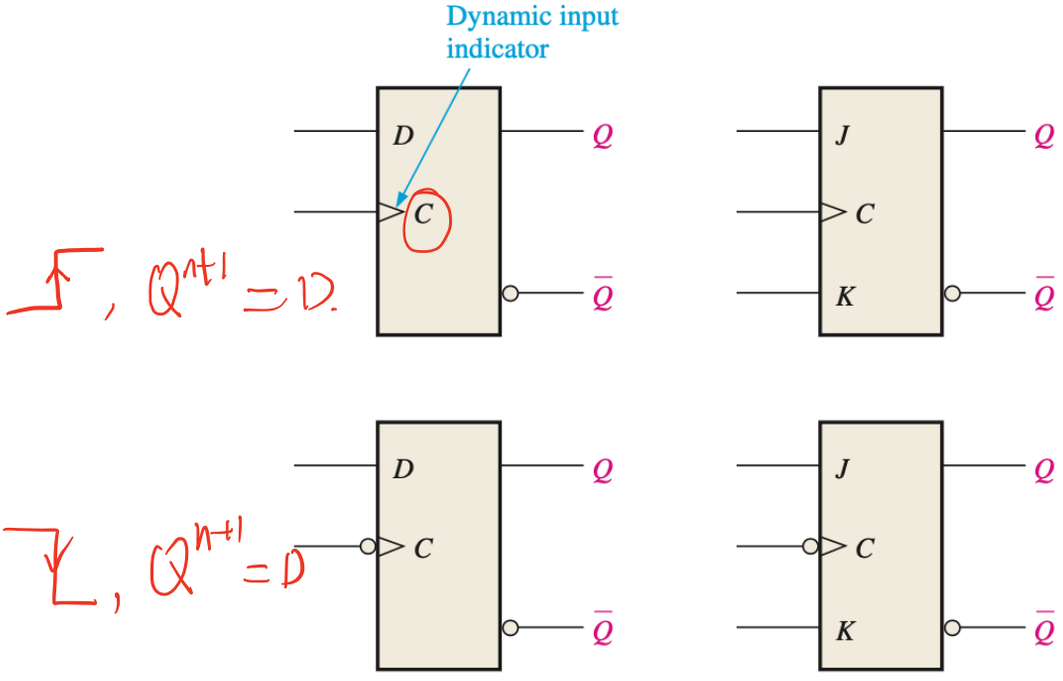
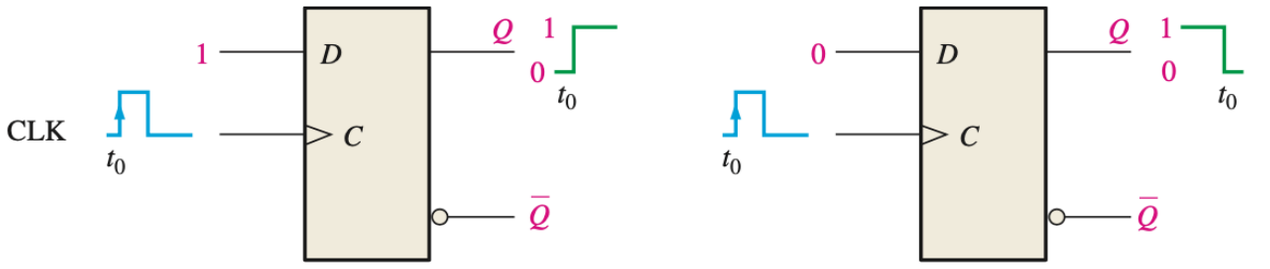


FIGURE 7–13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

The D Flip-Flop



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

FIGURE 7–14 Operation of a positive edge-triggered D flip-flop.

TABLE 7–2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

$Q^{n+1} = D$

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

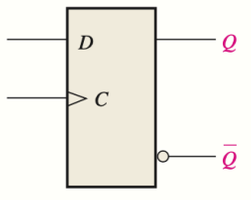


FIGURE 7–15

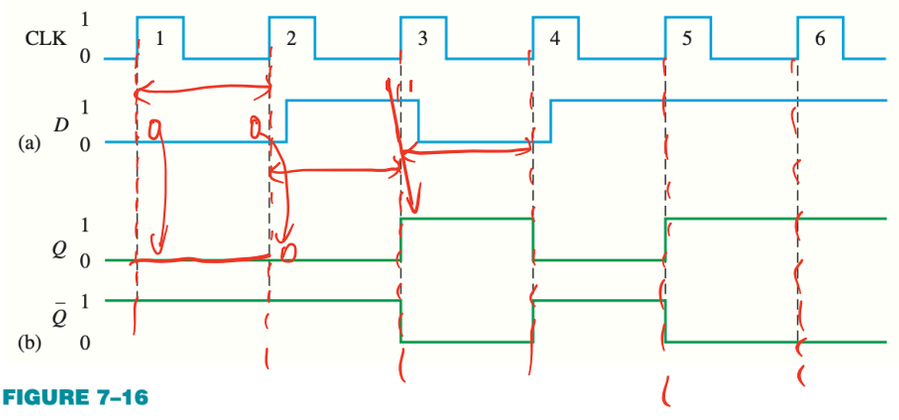
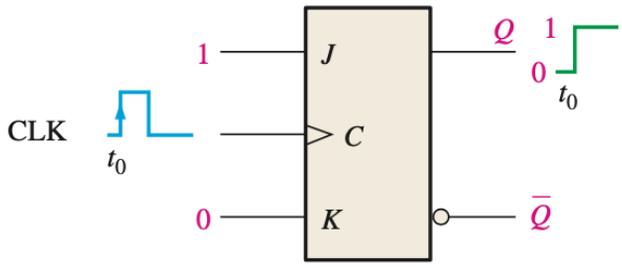
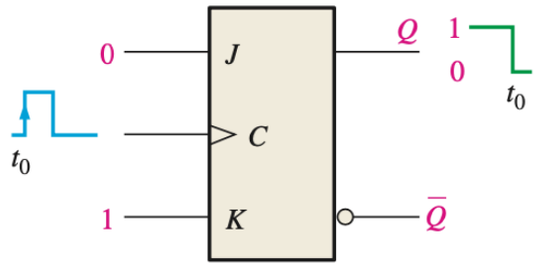


FIGURE 7–16

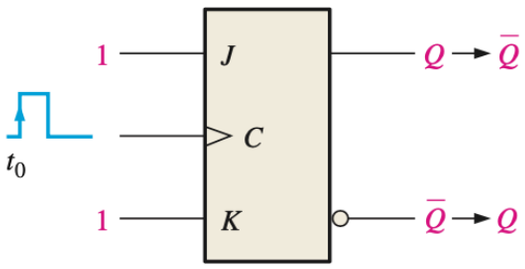
The J-K Flip-Flop



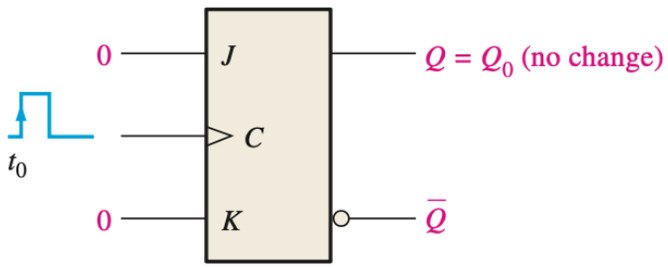
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

FIGURE 7–17 Operation of a positive edge-triggered J-K flip-flop.

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\bar{Q}$	Comments
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

$Q^{n+1} = \bar{Q}_n$

EXAMPLE 7–5

The waveforms in Figure 7–18(a) are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

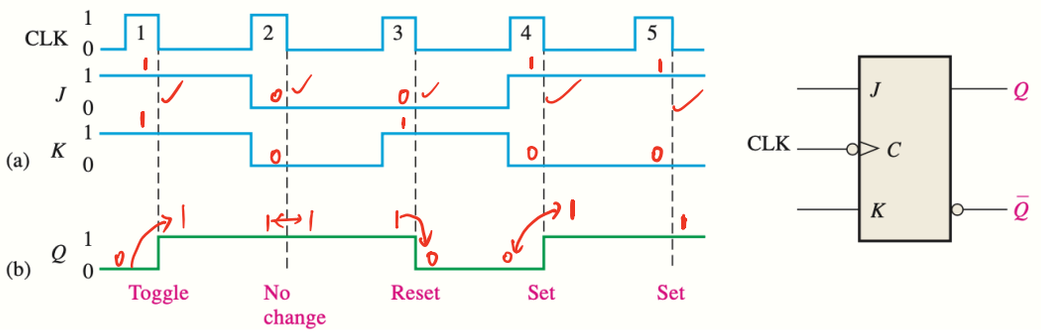
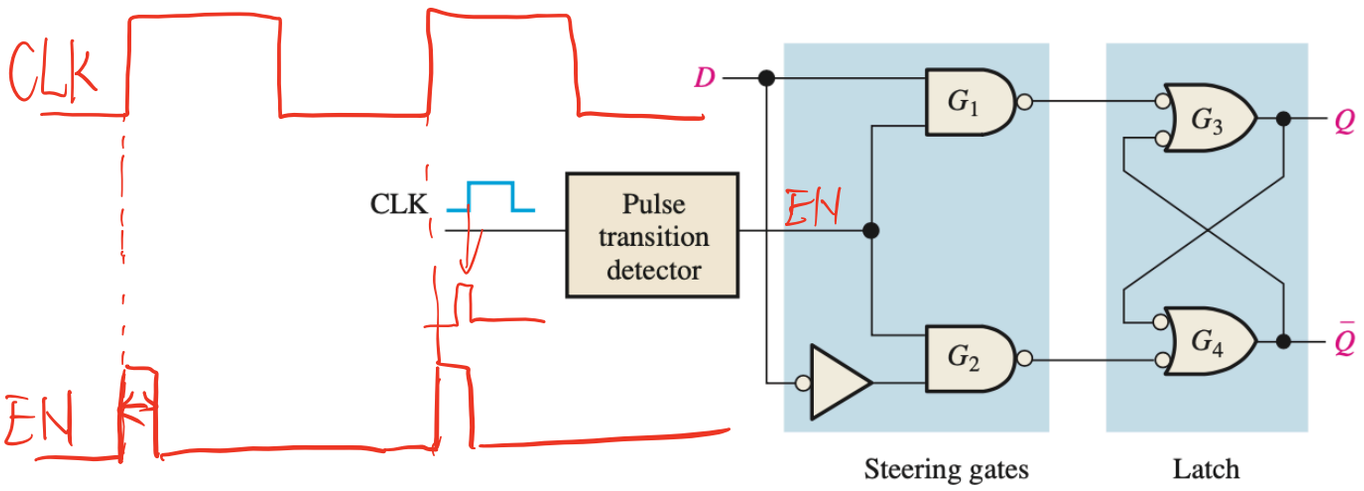
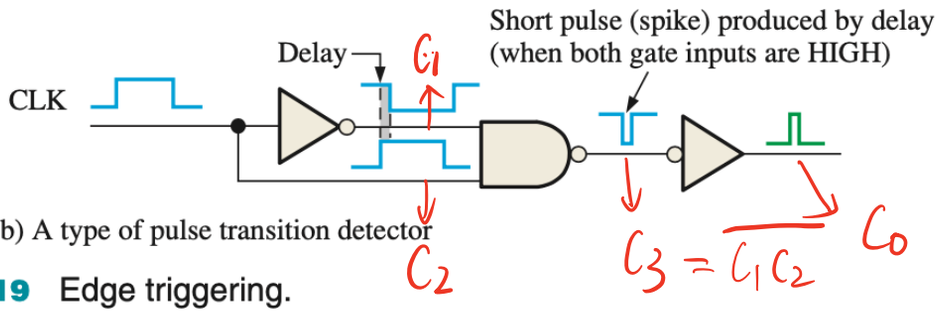


FIGURE 7–18

Edge-Triggered Operation-D Flip-Flop

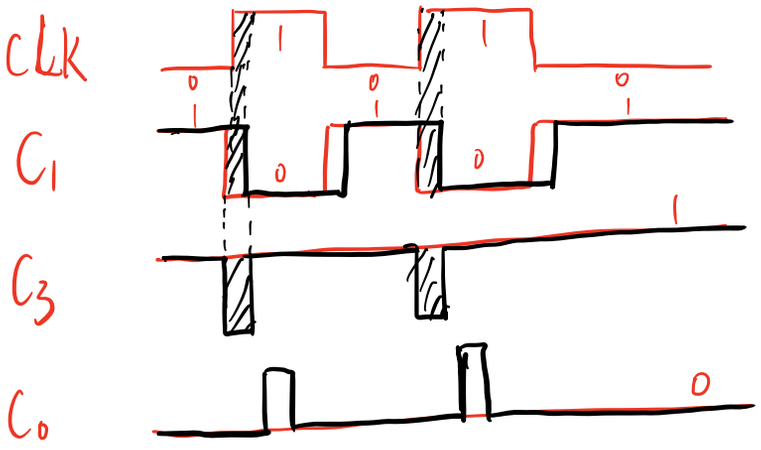


(a) A simplified logic diagram for a positive edge-triggered D flip-flop



(b) A type of pulse transition detector

FIGURE 7–19 Edge triggering.



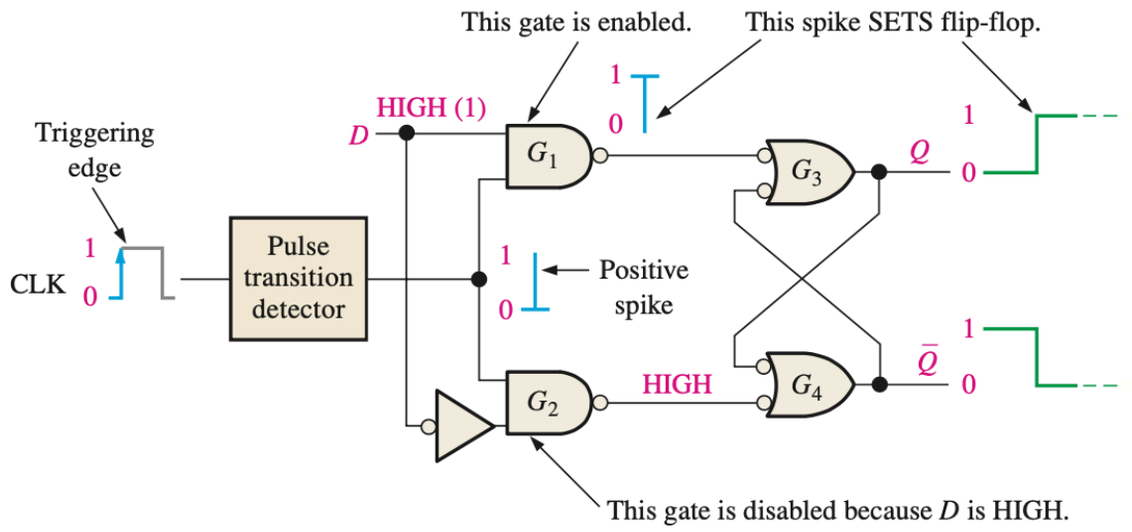


FIGURE 7–20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

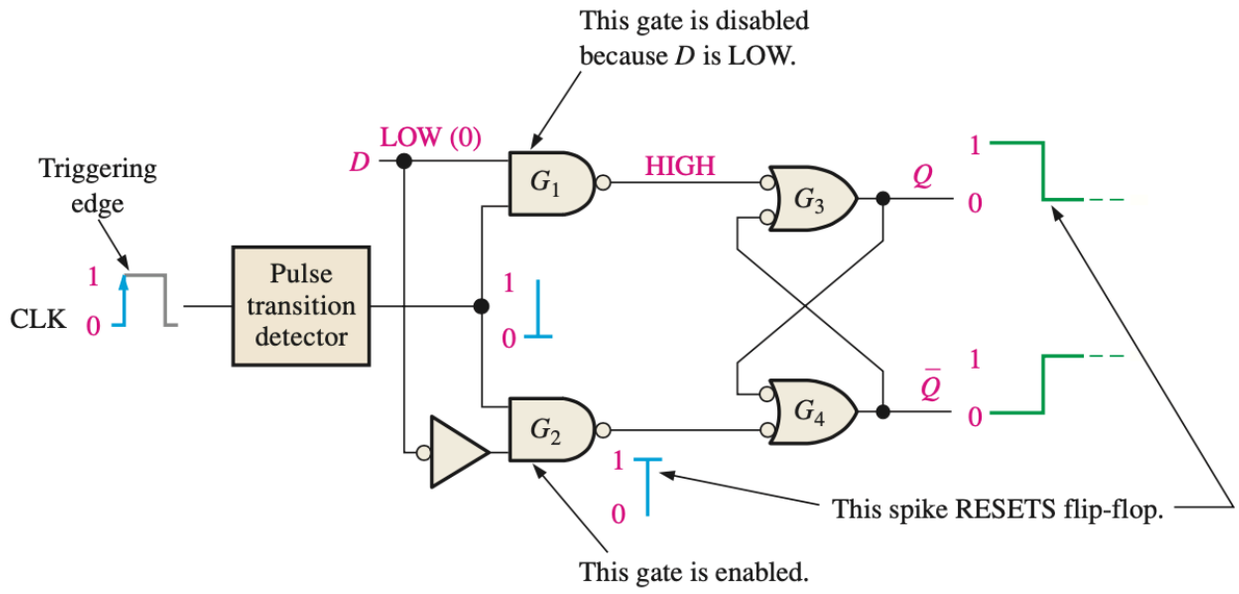


FIGURE 7–21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

EXAMPLE 7–6

Given the waveforms in Figure 7–22(a) for the *D* input and the clock, determine the *Q* output waveform if the flip-flop starts out RESET.

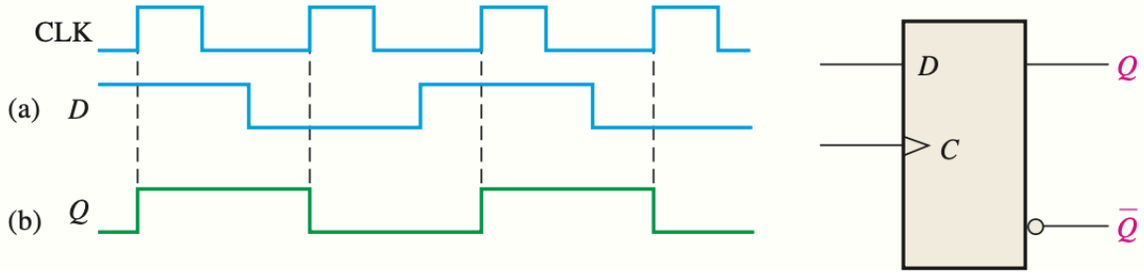
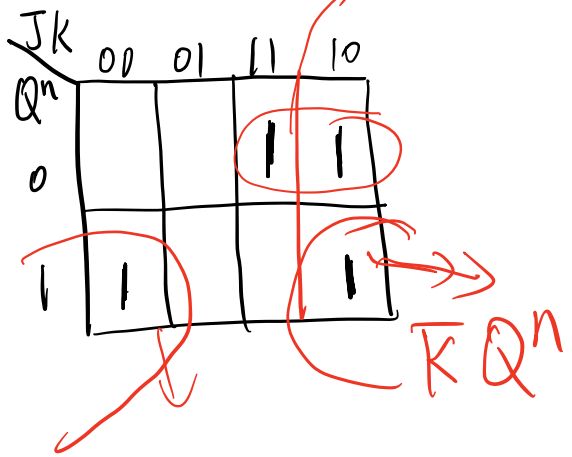


FIGURE 7–22

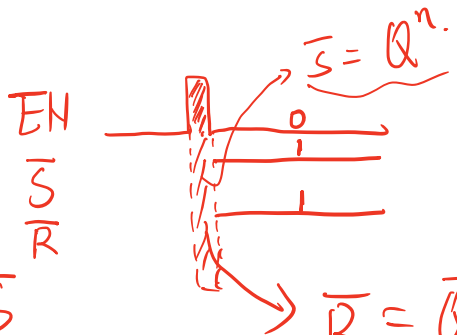
J	K	Q^n	Q^{n+1}
0	0	0	0 ✓
		1	0 ✓
0	1	0	0 ✓
		1	0
1	0	0	1 ✓
		1	1
1	1	0	1 ✓
		1	0

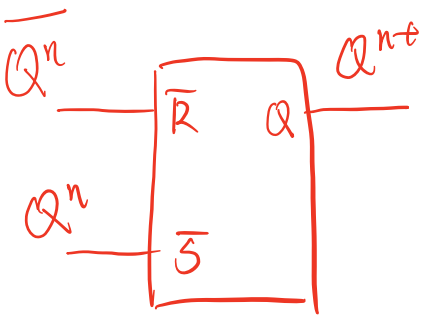
$$\bigstar \quad Q^{n+1} = J\overline{Q^n} + \overline{K}Q^n$$



$$Q^{n+1} = D_1$$

$$Q^{n+1} = \overline{R}S + \overline{R}Q^n$$





$\overline{R}$	$\overline{S}$	Q^n	Q^{n+1}
0	1	1	0
		0	0
1	0	1	1
		0	1

$\Rightarrow J=K=1, \quad Q^{n+1} = \overline{Q^n}$

J-K Flip-Flop

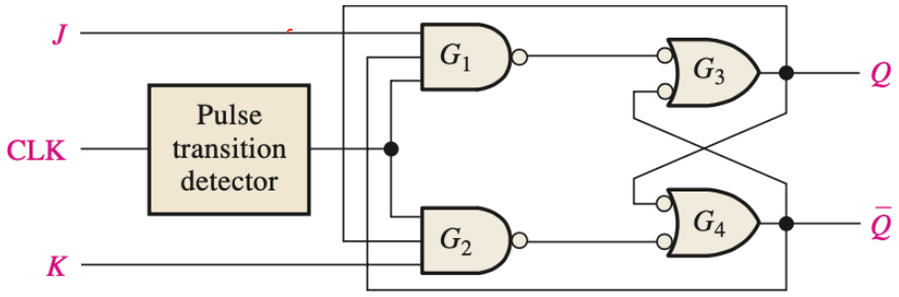


FIGURE 7–23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

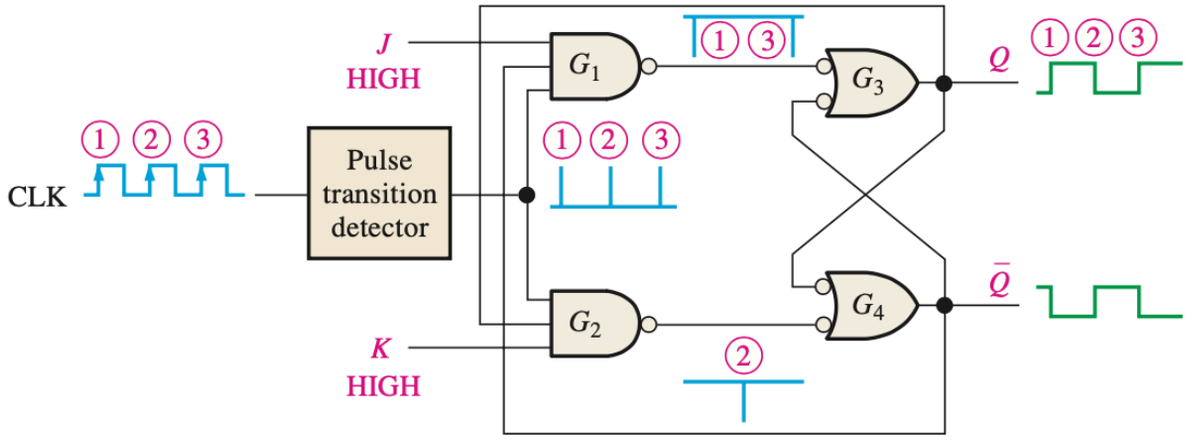


FIGURE 7–24 Transitions illustrating flip-flop operation.

Asynchronous Preset and Clear Inputs

input, D and the clock.

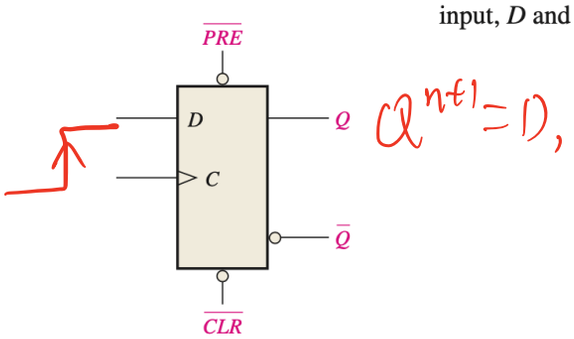


FIGURE 7–25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

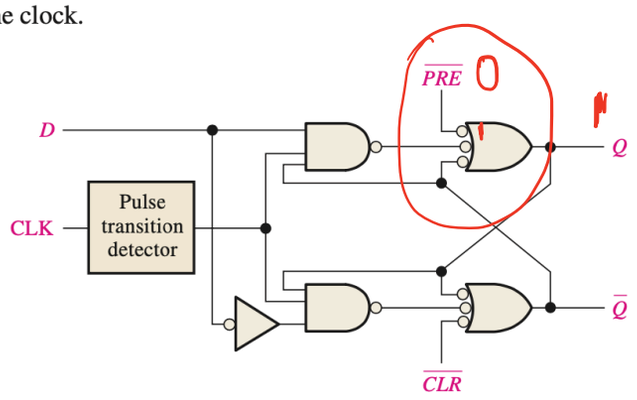


FIGURE 7–26 Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.

EXAMPLE 7–7

For the positive edge-triggered D flip-flop with preset and clear inputs in Figure 7–27, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.

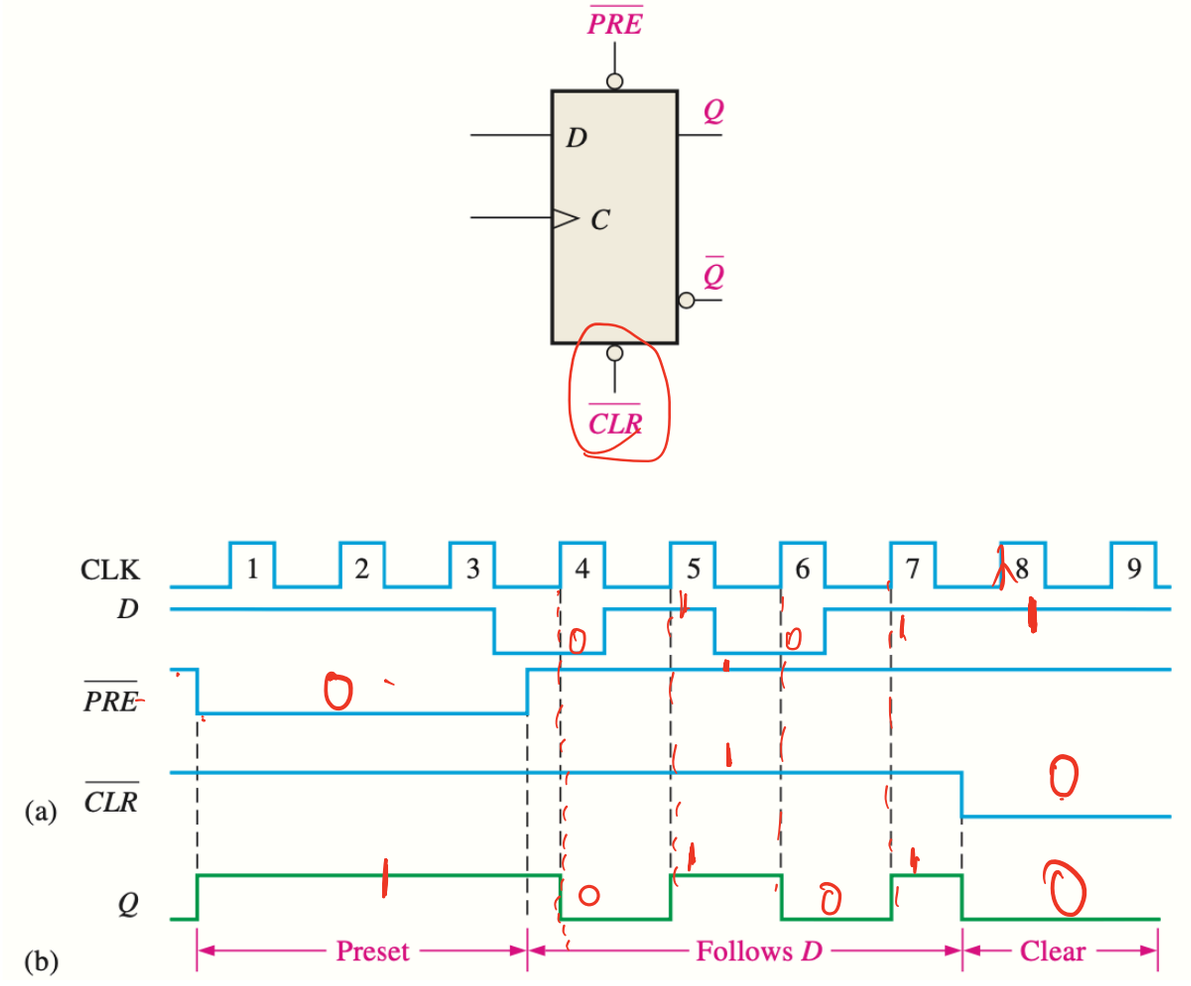
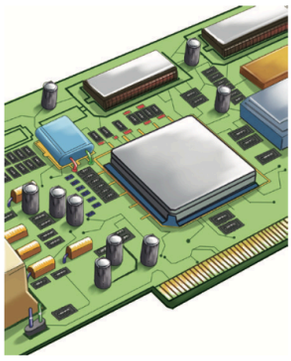
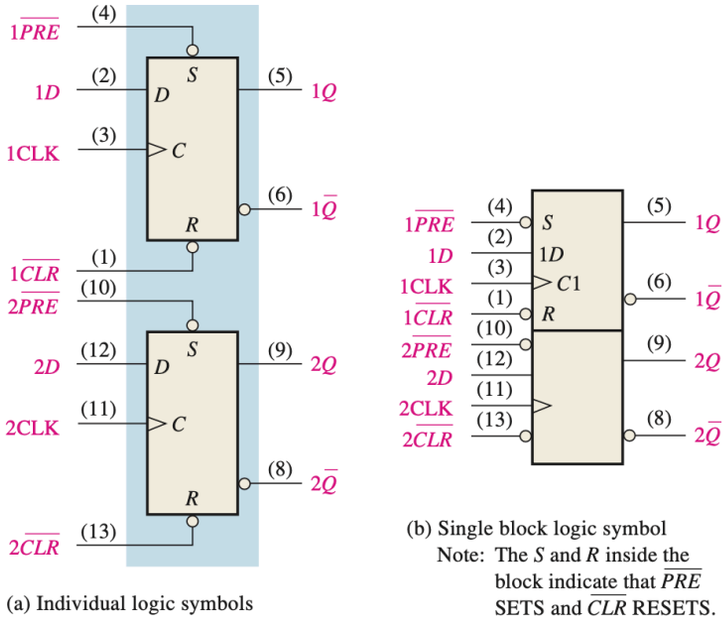


FIGURE 7–27 Open file F07-27 to verify the operation.

IMPLEMENTATION: D FLIP-FLOP



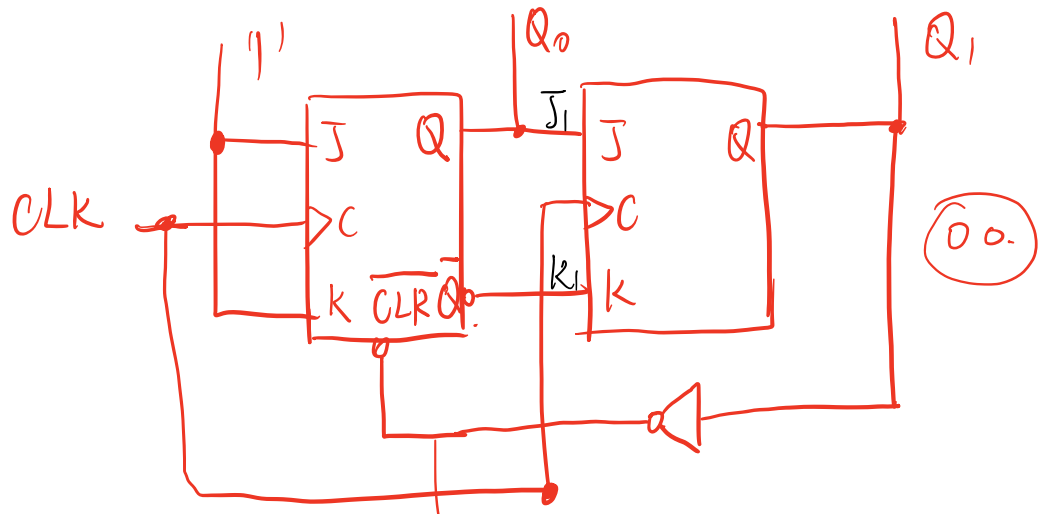
Fixed-Function Device The 74HC74 dual D flip-flop contains two identical D flip-flops that are independent of each other except for sharing V_{CC} and ground. The flip-flops are positive edge-triggered and have active-LOW asynchronous preset and clear inputs. The logic symbols for the individual flip-flops within the package are shown in Figure 7–28(a), and an ANSI/IEEE standard single block symbol that represents the entire device is shown in part (b). The pin numbers are shown in parentheses.

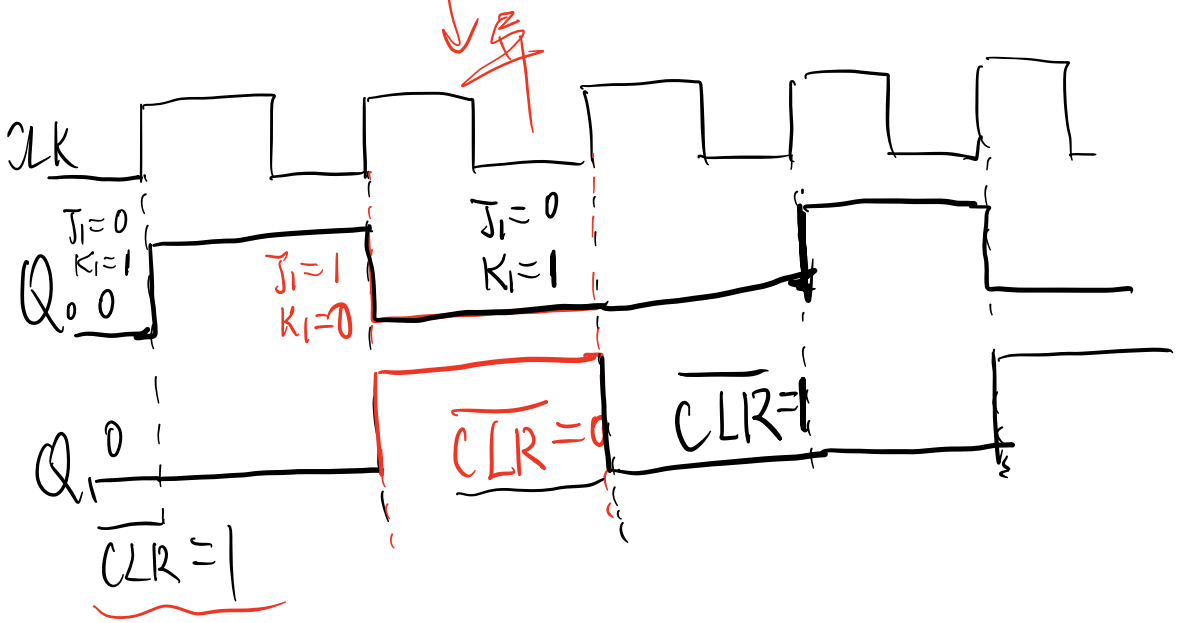


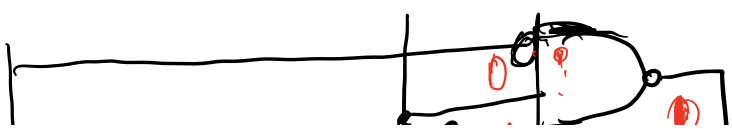
(a) Individual logic symbols

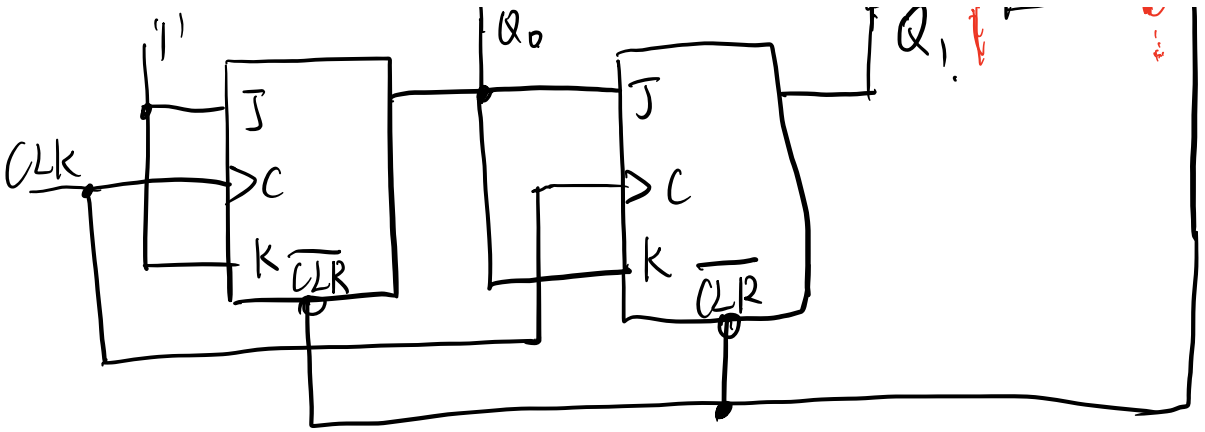
(b) Single block logic symbol
Note: The *S* and *R* inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS.

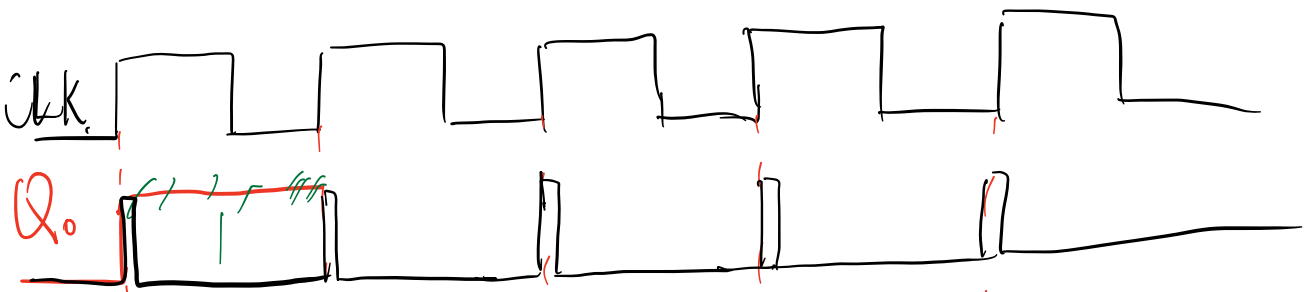
FIGURE 7–28 The 74HC74 dual positive edge-triggered D flip-flop.


'1'
Q_0
Q_1
J_1
J
Q
C
K
CLR
K_1
CLK
00.

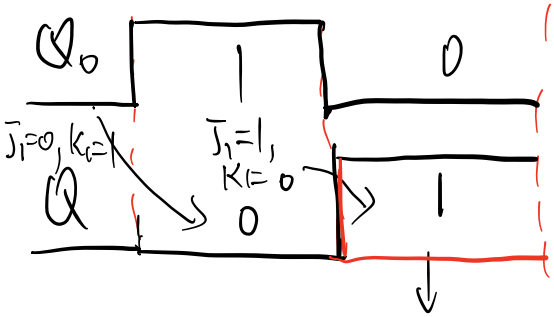

CLK
$J_1=0$
$K_1=1$
Q_0 0
$J_1=1$
$K_1=0$
$J_1=0$
$K_1=1$
Q_1 0
$\overline{CLR}=0$
$\overline{CLR}=1$
$\overline{CLR}=1$

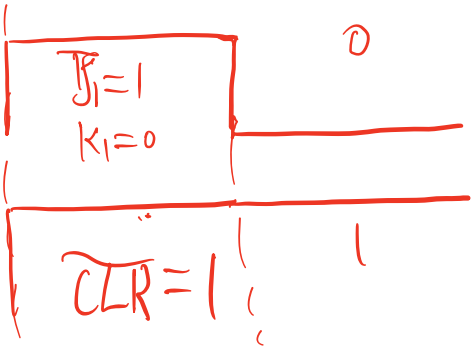

0

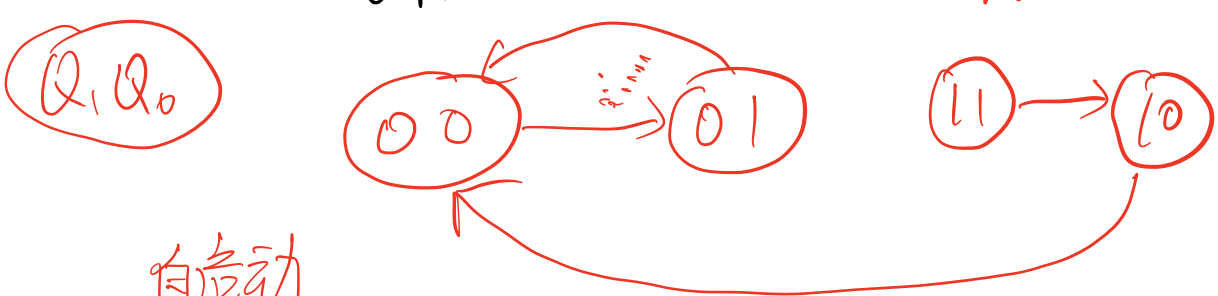

'1'
J
C
K
CLR
Q_0
Q_1
CLK


CLK
Q_0


Q_1
0


Q_0
1
0
$J_1=0, K_1=1$
$J_1=1, K_1=0$
$\overline{Q}$
0
1
$\overline{CLR}=0$


$J_1=1$
$K_1=0$
0
$\overline{CLR}=1$
1


Q_1Q_0
00
01
11
10

自启动

EXAMPLE 7–8

The 1J, 1K, 1CLK, 1$\overline{PRE}$, and 1$\overline{CLR}$ waveforms in Figure 7–30(a) are applied to one of the negative edge-triggered flip-flops in a 74HC112 package. Determine the 1Q output waveform.

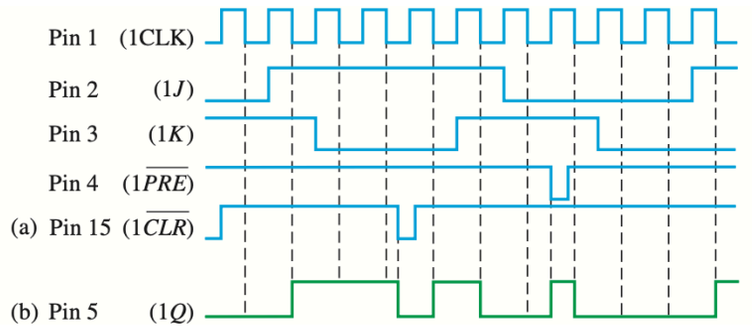
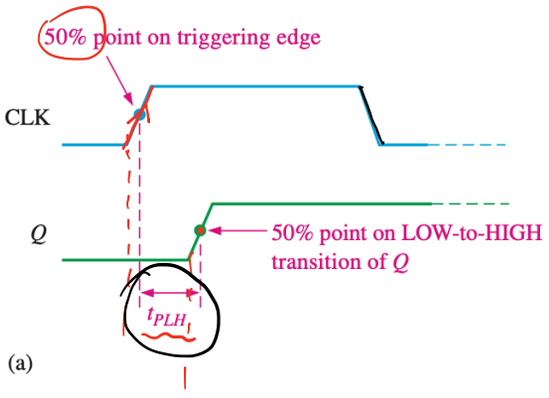


FIGURE 7–30

7-3 Flip-Flop Operating Characteristics

Propagation Delay Times



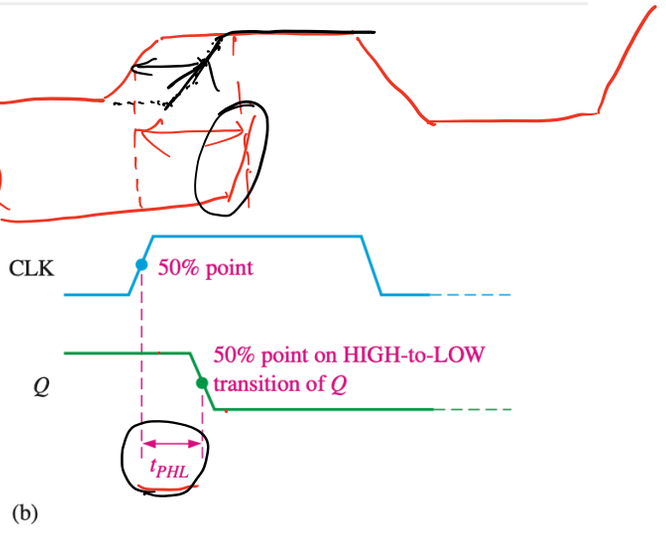
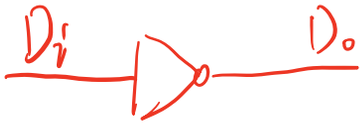
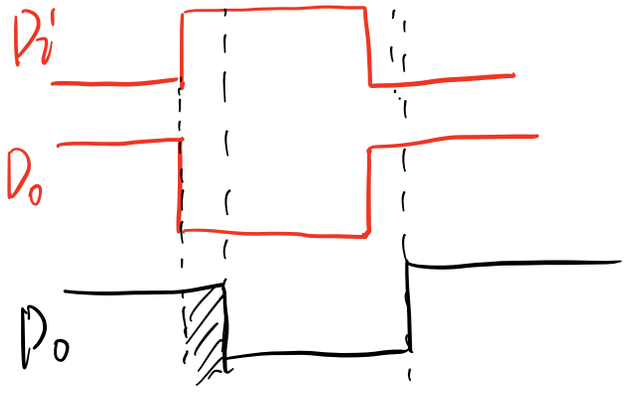


FIGURE 7–31 Propagation delays, clock to output.





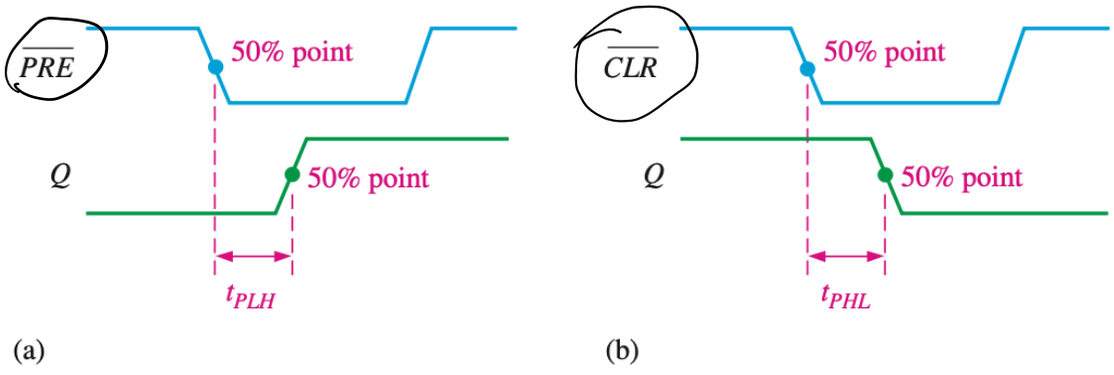


FIGURE 7–32 Propagation delays, preset input to output and clear input to output.

Set-up Time

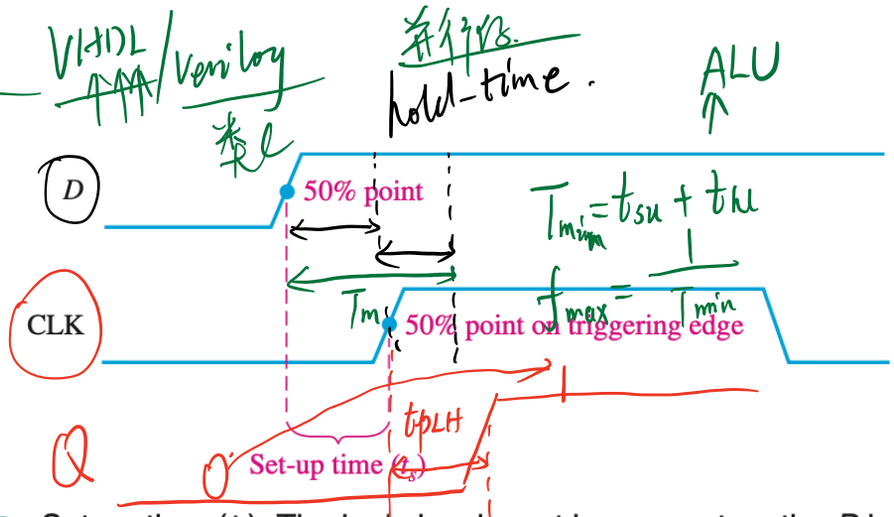


FIGURE 7–33 Set-up time (t_s). The logic level must be present on the *D* input for a time equal to or greater than t_s before the triggering edge of the clock pulse for reliable data entry.

Hold Time

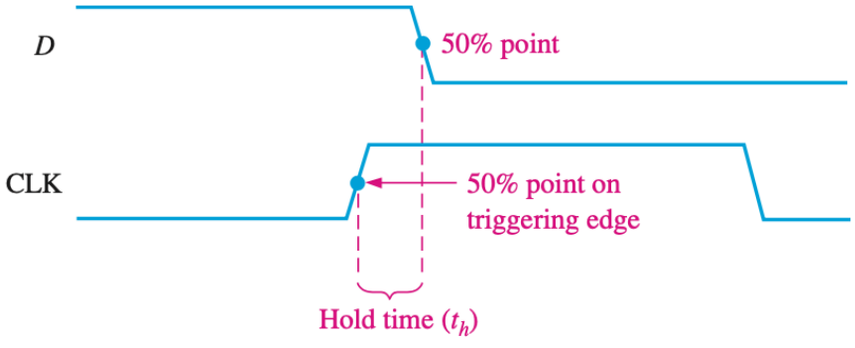


FIGURE 7–34 Hold time (t_h). The logic level must remain on the *D* input for a time equal to or greater than t_h after the triggering edge of the clock pulse for reliable data entry.

Maximum Clock Frequency

Pulse Widths

Power Dissipation

$$P = V_{CC} * I_{CC}$$

Comparison of Specific Flip-Flops

TABLE 7–4

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

	CMOS		Bipolar (TTL)	
Parameter	**74HC74A**	**74AHC74**	**74LS74A**	**74F74**
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
t_{PHL} ($\overline{CLR}$ to Q)	18 ns	4.8 ns	40 ns	9.0 ns
t_{PLH} ($\overline{PRE}$ to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_W (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_W (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
t_W ($\overline{CLR}$/$\overline{PRE}$)	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

7–4 Flip-Flop Applications

Parallel Data Storage

2+1=3ns

$\frac{1}{3} \approx 330\,MHz$

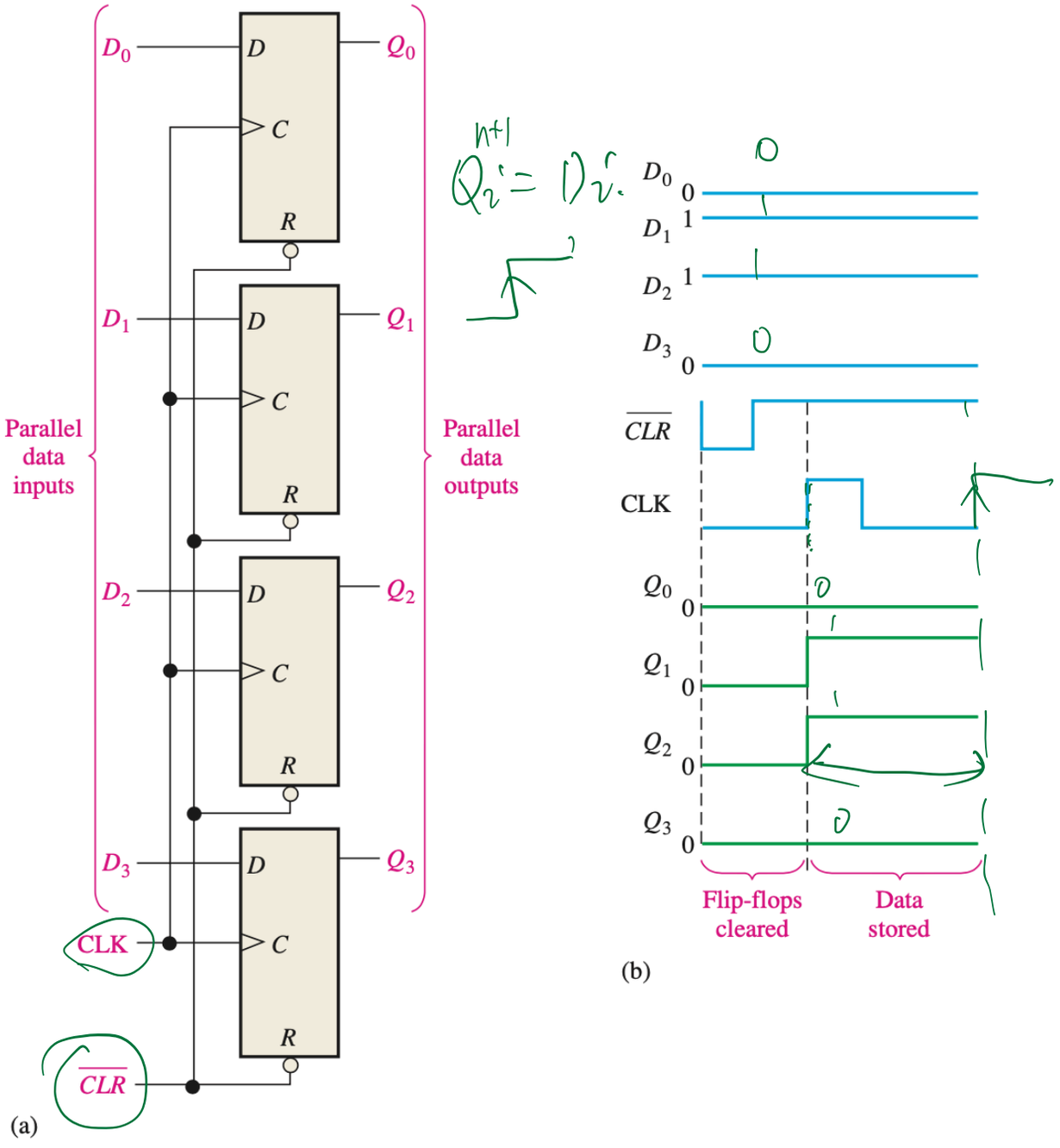


FIGURE 7–35 Example of flip-flops used in a basic register for parallel data storage.

Frequency Division

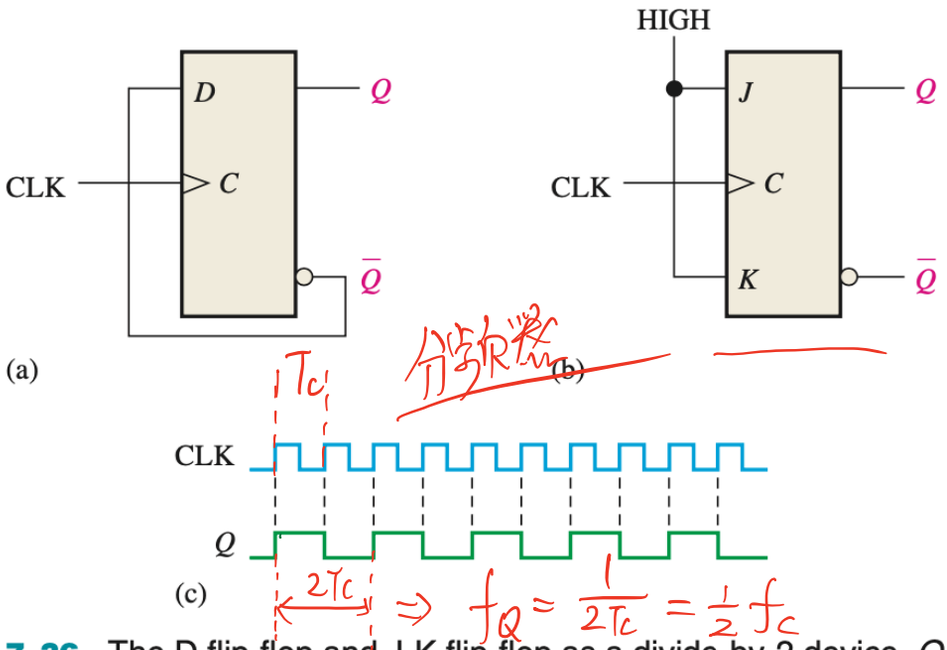


FIGURE 7–36 The D flip-flop and J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK. Open file F07-36 and verify the operation.

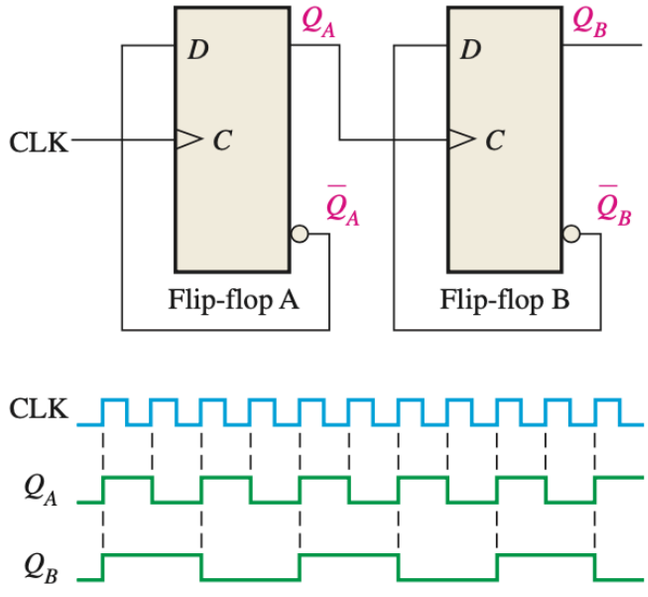
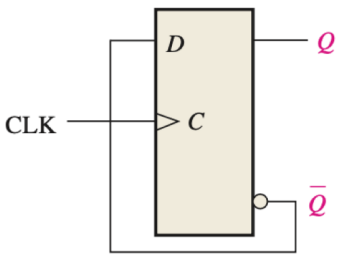
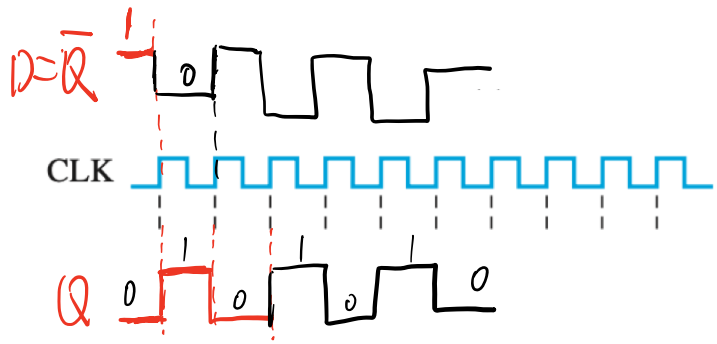


FIGURE 7–37 Example of two D flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK. Open file F07-37 and verify the operation.

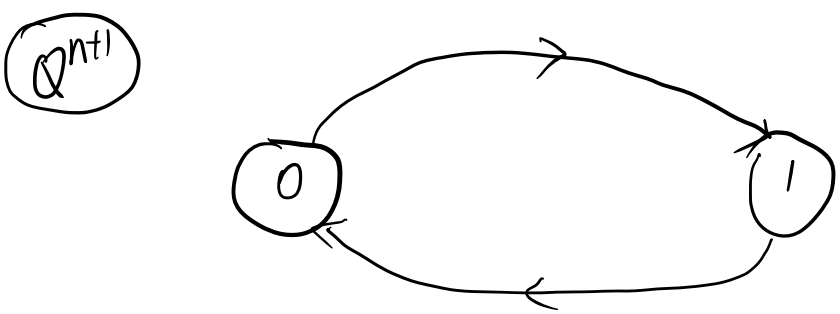


(a)



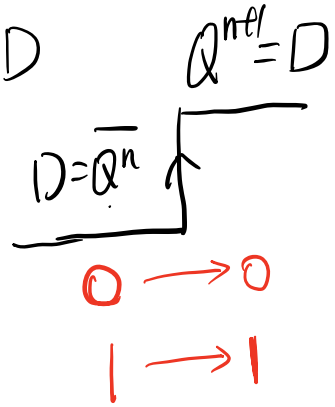
$Q^{n+1} = D$, $D = \overline{Q^n}$ $Y = Q^{n+1}$

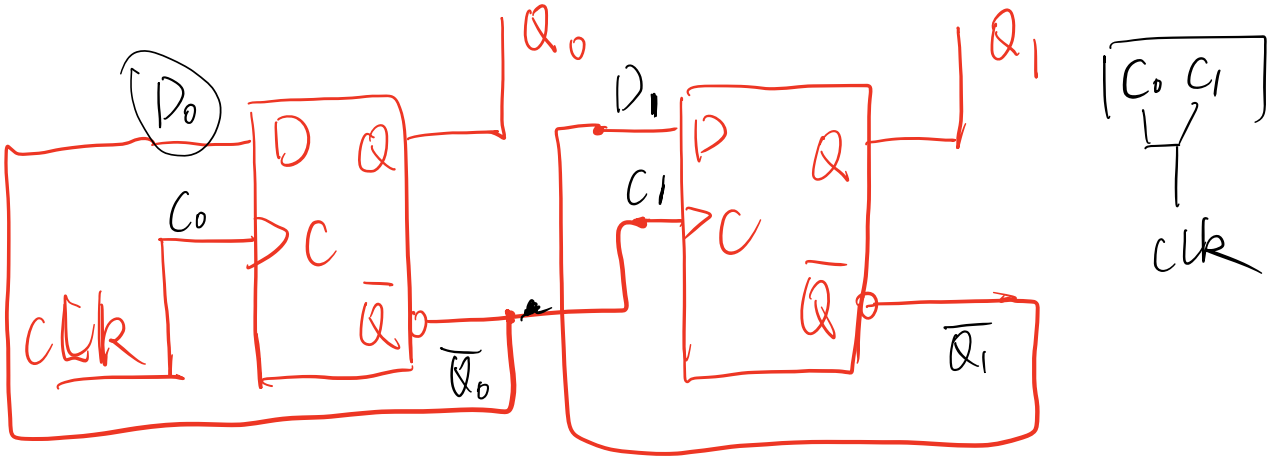
① 状态, ② 转换方程, ③ 转换输出方程

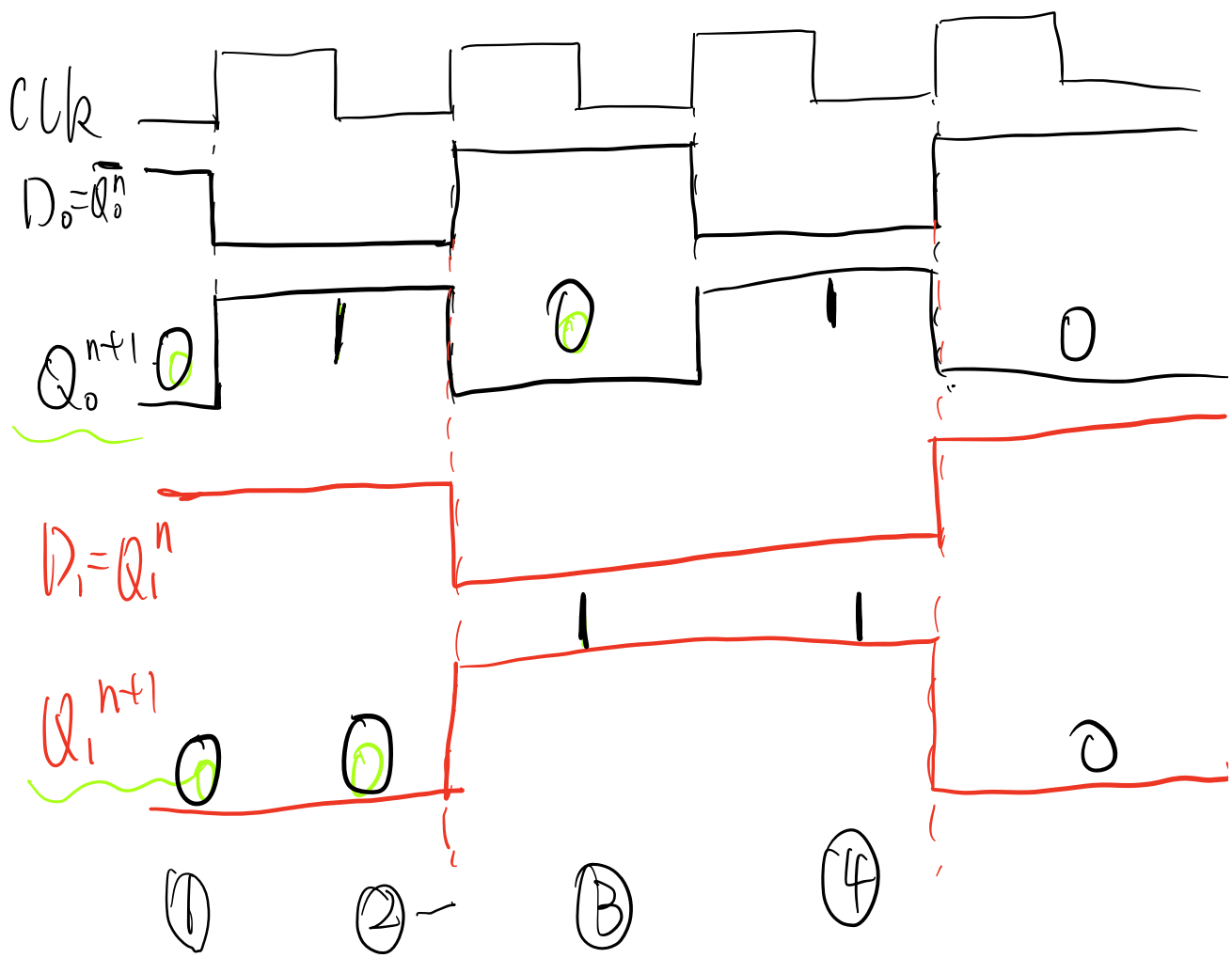


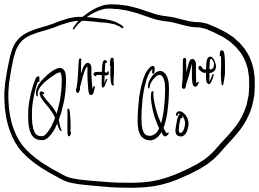
状态图

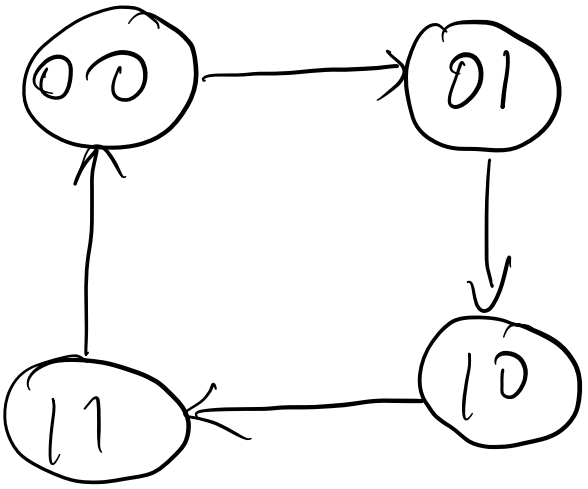
CLK	$D=\overline{Q^n}$	$Q^{n+1}=D$
↑	0 ($\overline{Q^n}=1$)	0
	1 ($\overline{Q^n}=0$)	1




Q_0
Q_1
D_0
D_1
D
Q
C
$\bar{Q}$
C_0
C_1
CLK
$\bar{Q}_0$
$\bar{Q}_1$
C_0 C_1
CLK


CLK
$D_0 = \bar{Q}_0^n$
Q_0^{n+1}
0
1
0
0
$D_1 = Q_1^n$
Q_1^{n+1}
0
0
0
1
2
3
4

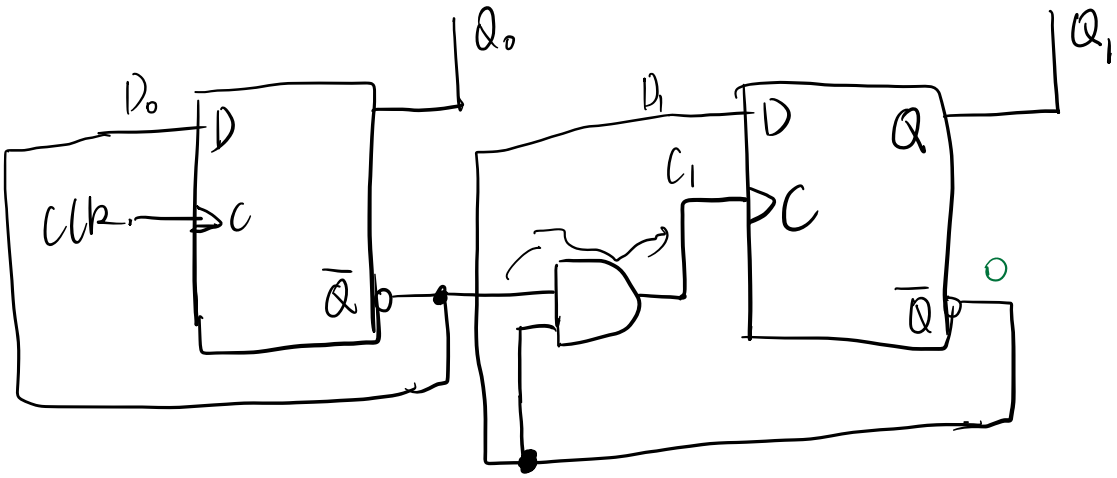


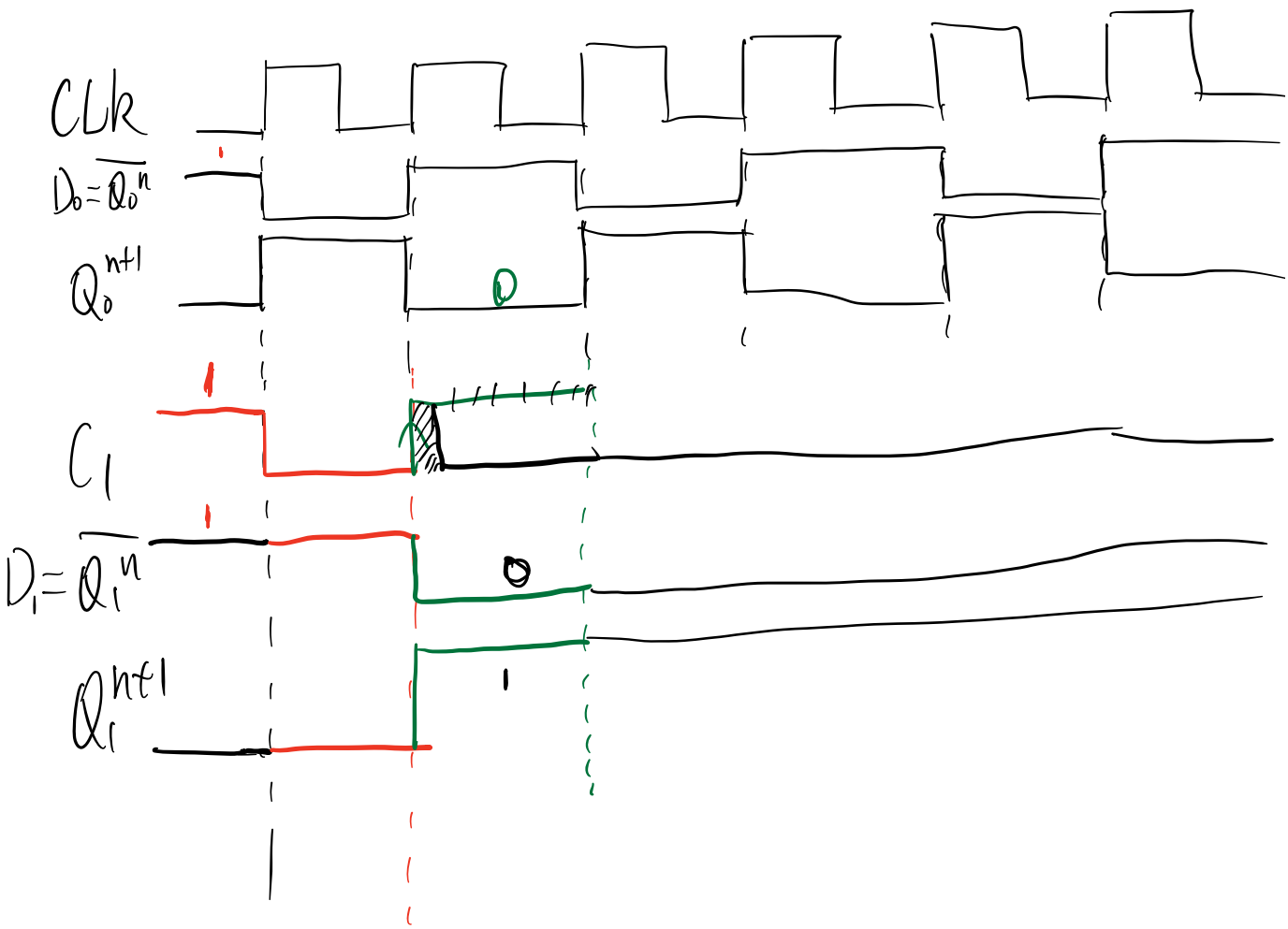


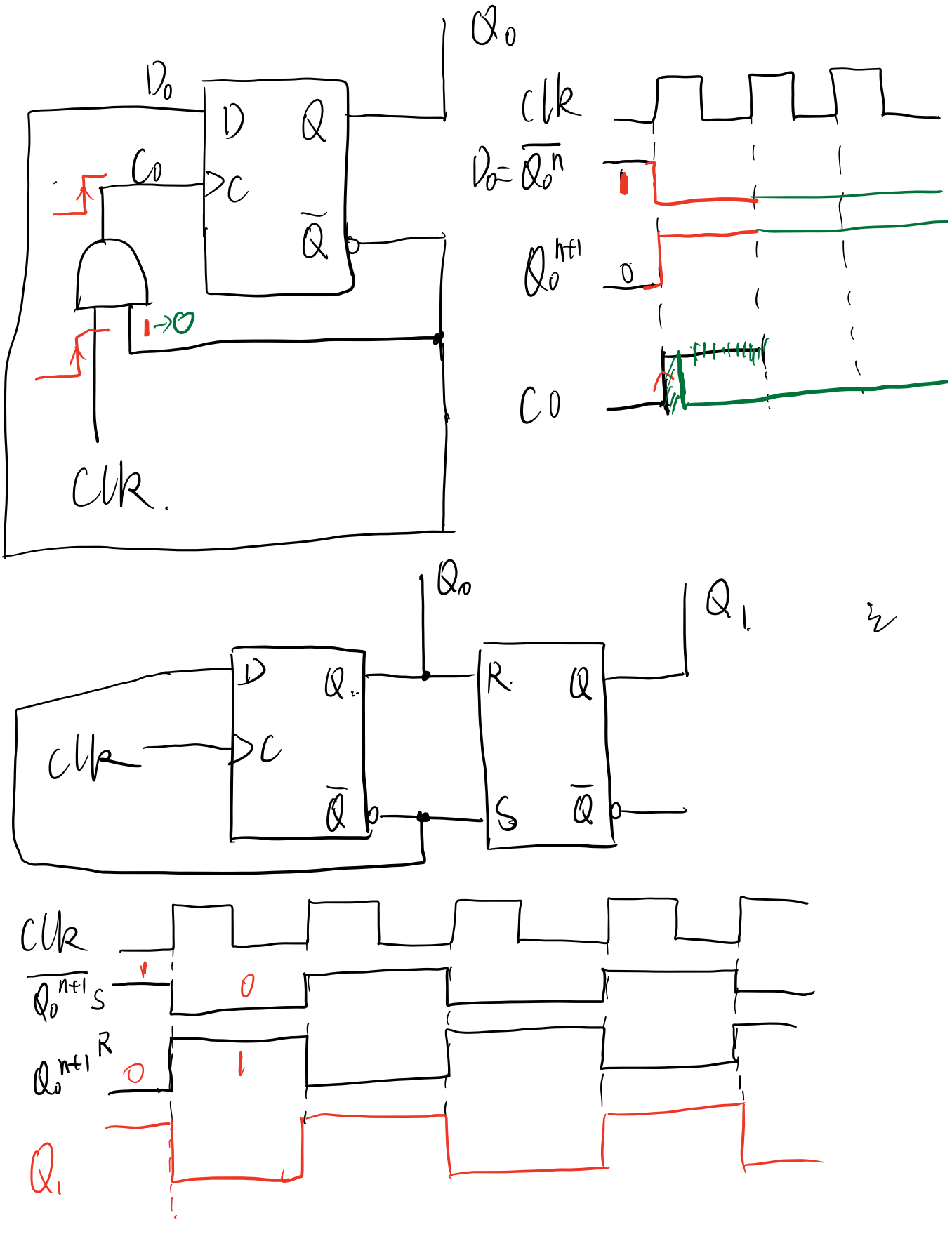
状态：
$$\begin{cases} Q_0^{n+1} = D_0, \\ Q_1^{n+1} = D_1, \end{cases}$$

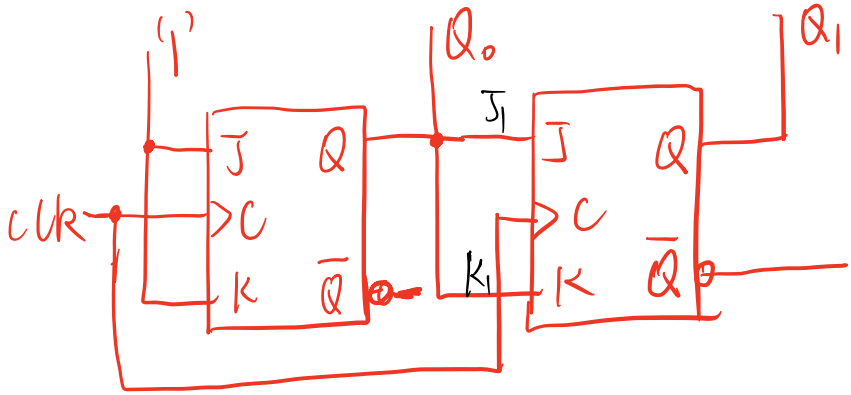
输入：
$$\begin{cases} D_0 = \overline{Q_0^n} \\ D_1 = \overline{Q_1^n} \end{cases}$$

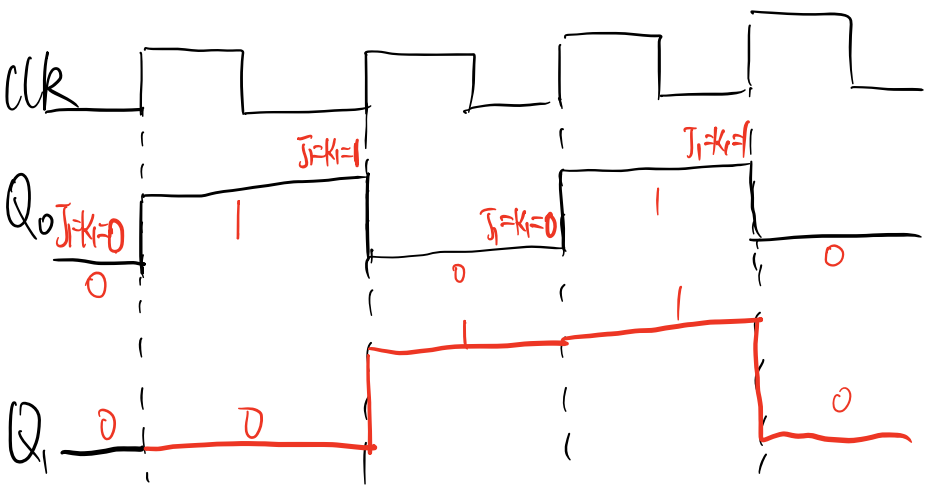
输出：Q_1^{n+1} Q_0^{n+1}.

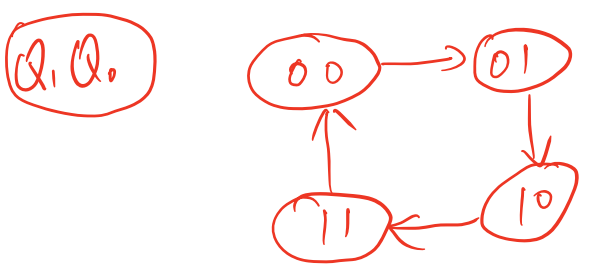

Q_0
Q_1
D_0
D
CLK
C
$\overline{Q}$
D_1
D
Q
C_1
C
$\overline{Q}$
0


CLK
$D_0 = \overline{Q_0}^n$
Q_0^{n+1}
0
C_1
$D_1 = \overline{Q_1}^n$
0
Q_1^{n+1}
1


Q0
D0
D
Q
C0
C
Q̄
1→0
CLK.
CLK
D0= Q̄0n
Q0n+1
0
C0
Q0
Q1
2
D
Q
CLK
C
Q̄
R
Q
S
Q̄
CLK
Q0n+1 S
1
0
Q0n+1 R
0
1
Q1


'1'
Q_0
Q_1
J_1
J
Q
C
K
$\bar{Q}$
CLK
K_1


CLK
Q_0
Q_1
$J=K=1$
$J=K=0$
$J_1=K_1=1$
$J_1=K_1=0$
0
1


Q_1Q_0
00
01
10
11

EXAMPLE 7–9

Develop the f_{out} waveform for the circuit in Figure 7–38 when an 8 kHz square wave input is applied to the clock input of flip-flop A.

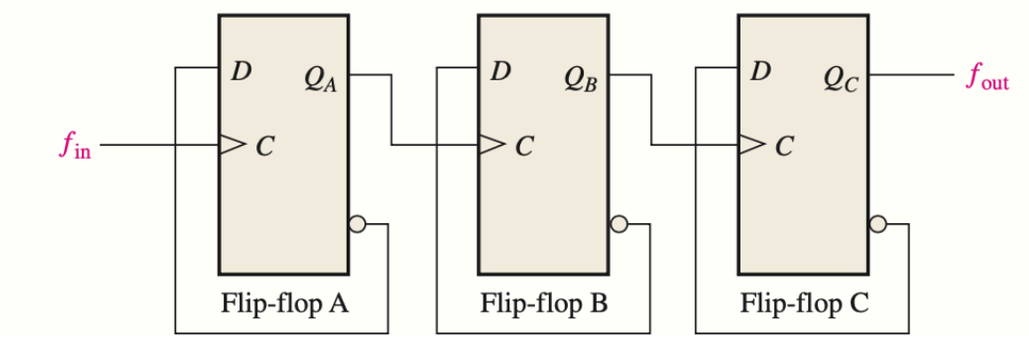
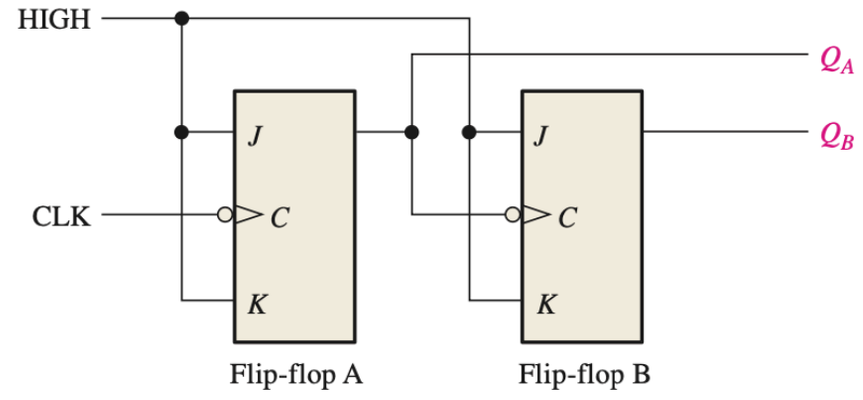


FIGURE 7–38

Counting



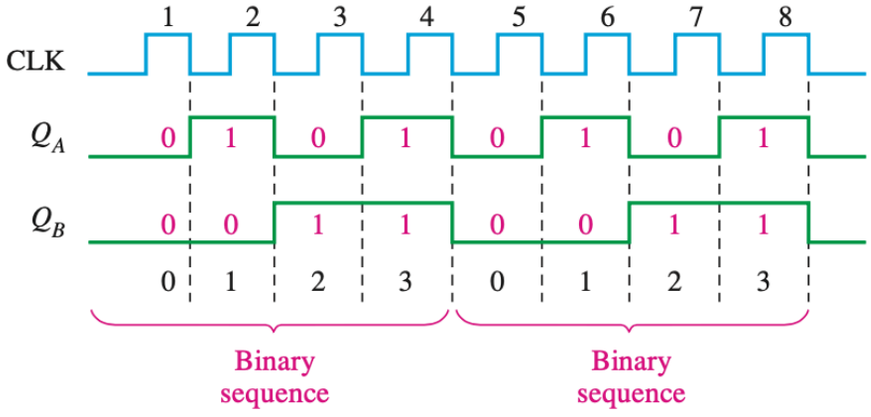


FIGURE 7–40 J-K flip-flops used to generate a binary count sequence (00, 01, 10, 11). Two repetitions are shown.

EXAMPLE 7–10

Determine the output waveforms in relation to the clock for Q_A, Q_B, and Q_C in the circuit of Figure 7–41 and show the binary sequence represented by these waveforms.

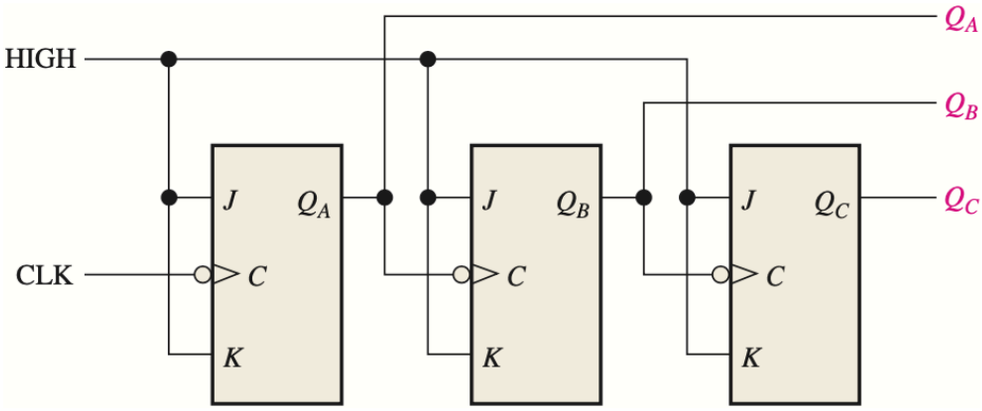


FIGURE 7–41

7–5 One-Shots

The **one-shot**,** also known as a **monostable** multivibrator, is a device with only one stable state. A one-shot is normally in its stable state and will change to its unstable state only when triggered. Once it is triggered, the one-shot remains in its unstable state for a prede- termined length of time and then automatically returns to its stable state. The time that the device stays in its unstable state determines the pulse width of its output.

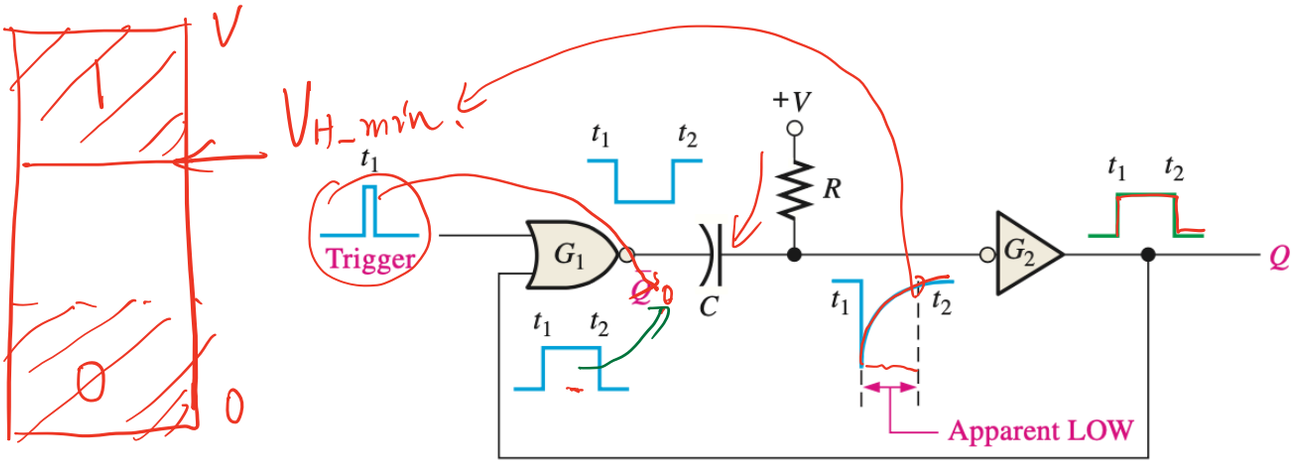
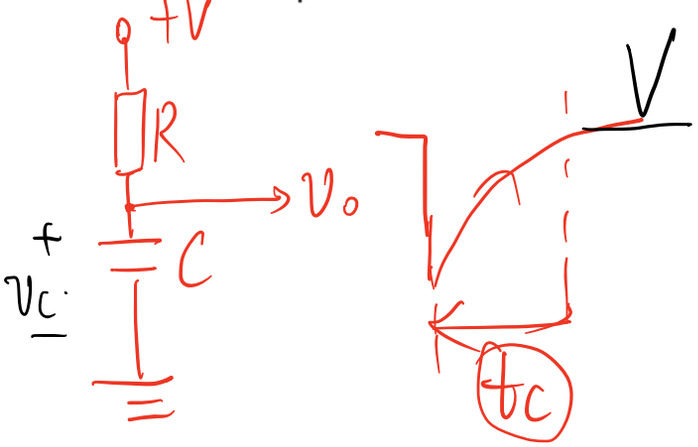


FIGURE 7–43 A simple one-shot circuit.



$$V_C(0+) = V_C(0-) = 0\,V$$

$$V_C(\infty) = V$$

$$\tau = RC$$

$$v_C(t) = V_C(\infty) + [V_C(0+) - V_C(\infty)]e^{-\frac{t}{\tau}}$$

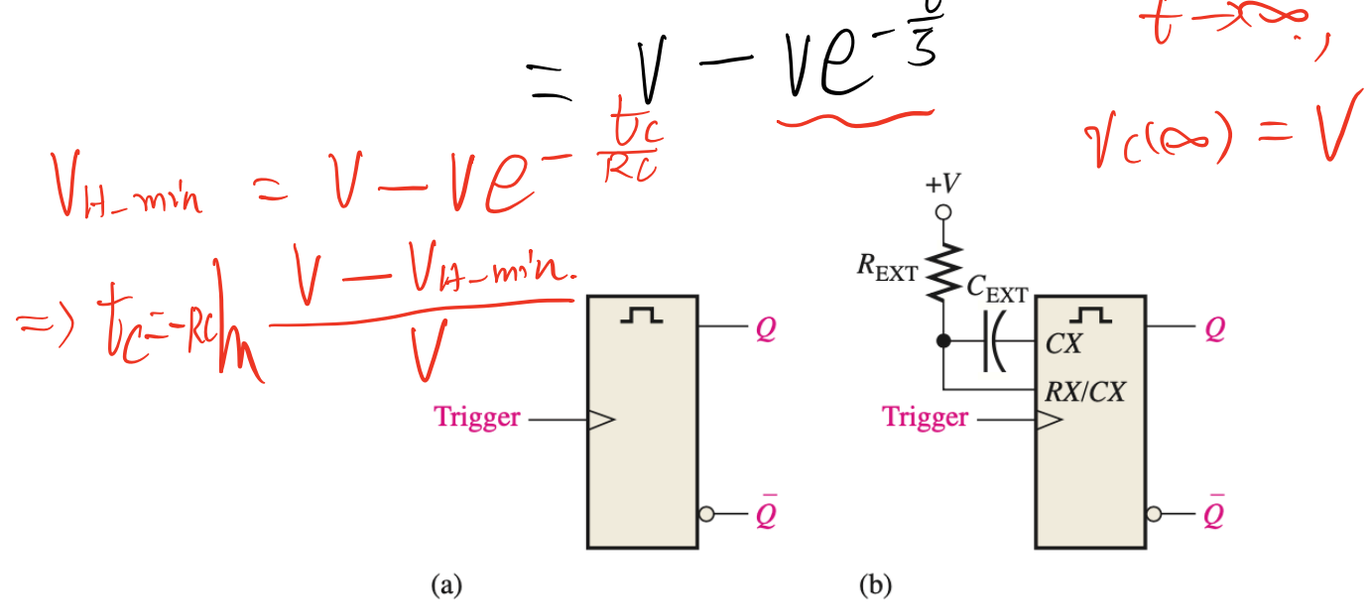


FIGURE 7–44 Basic one-shot logic symbols. *CX* and *RX* stand for external components.

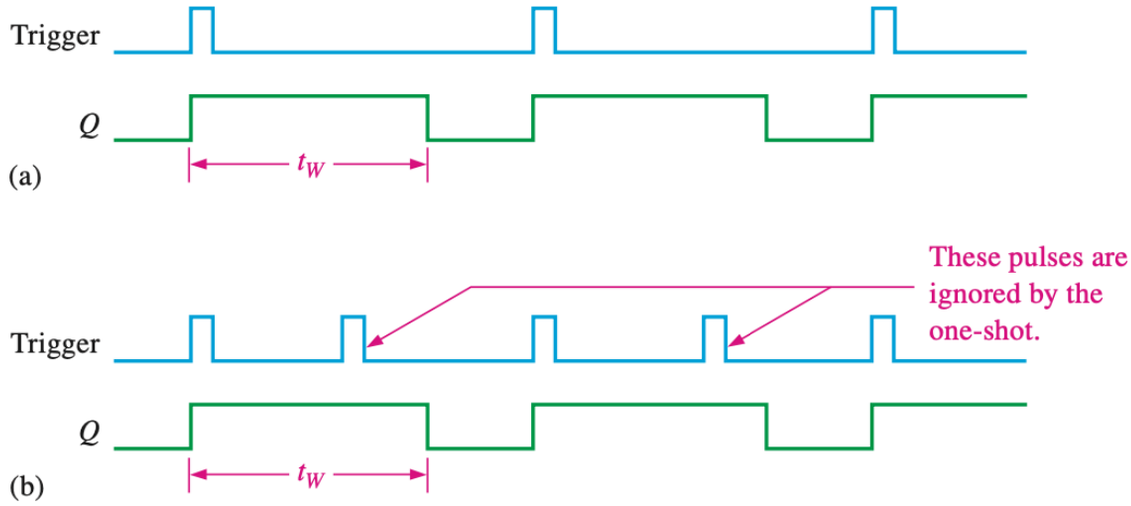


FIGURE 7–45 Nonretriggerable one-shot action.

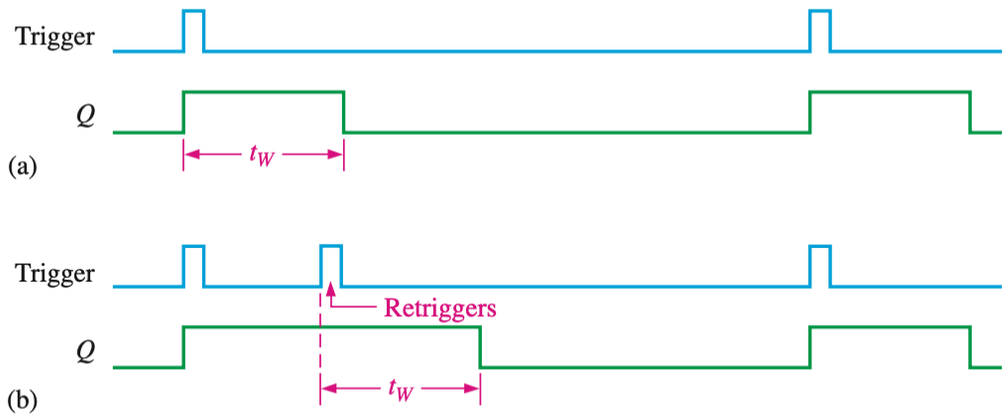


FIGURE 7–46 Retriggerable one-shot action.

Nonretriggerable One-Shot

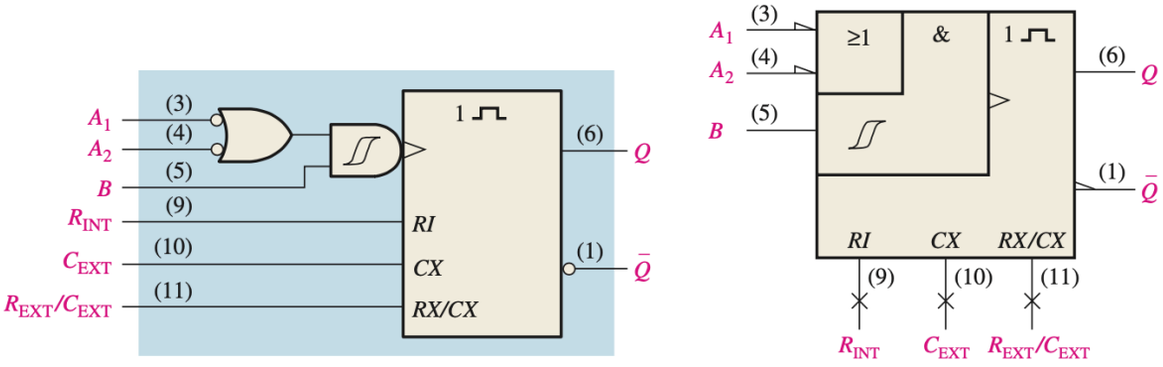


FIGURE 7–47 Logic symbols for the 74121 nonretriggerable one-shot.

The 555 Timer as a One-Shot

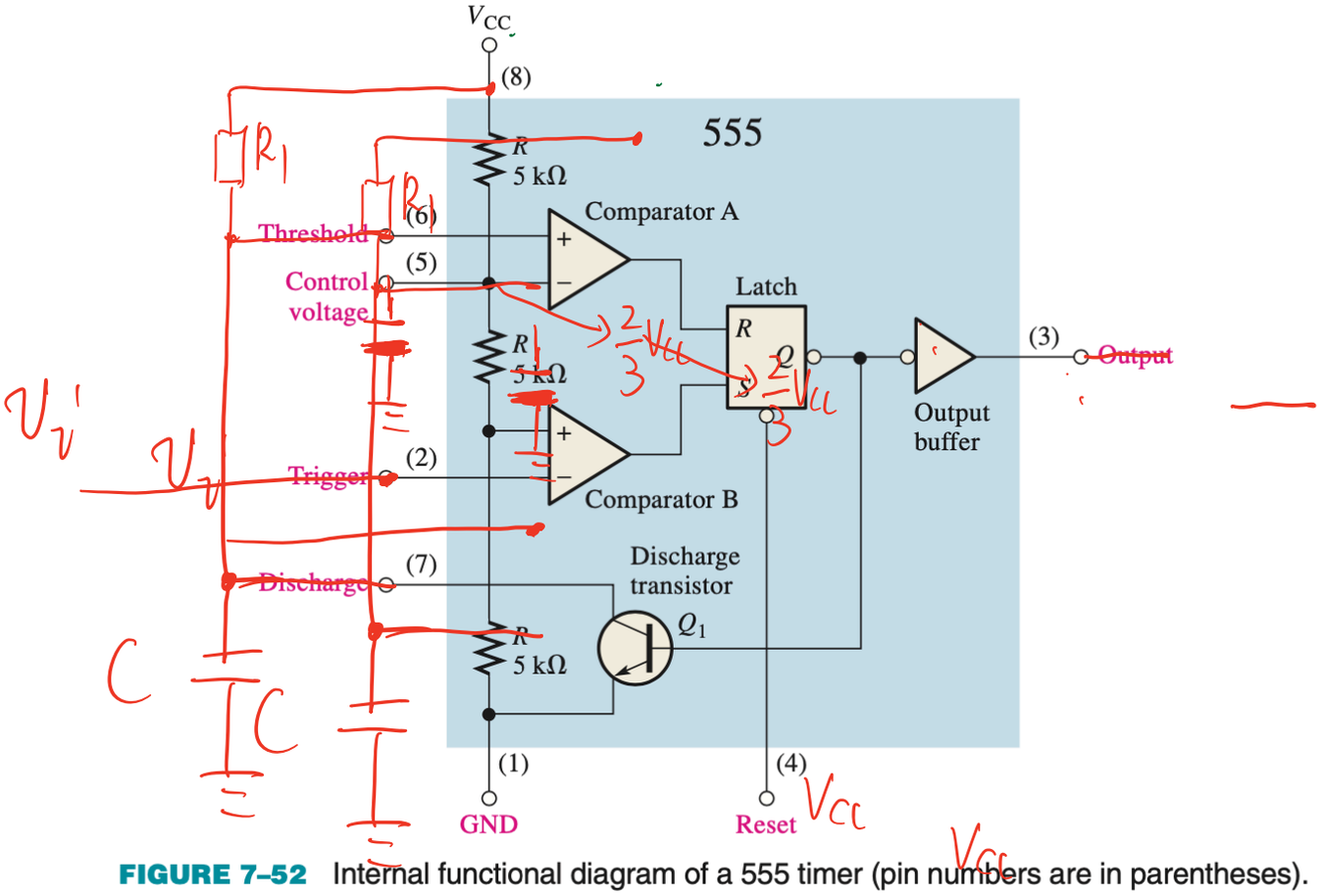


FIGURE 7–52 Internal functional diagram of a 555 timer (pin numbers are in parentheses).

Monostable (One-Shot) Operation

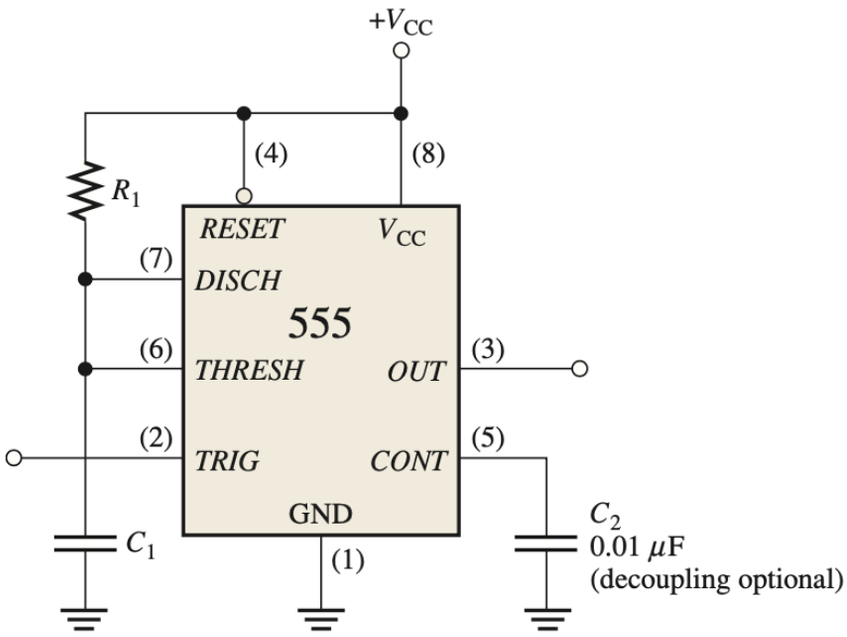
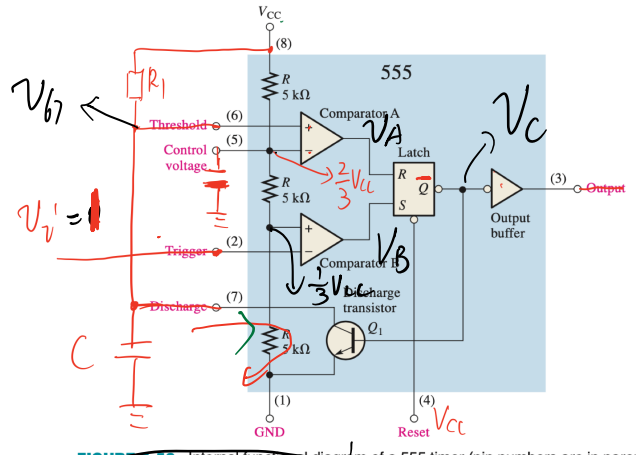
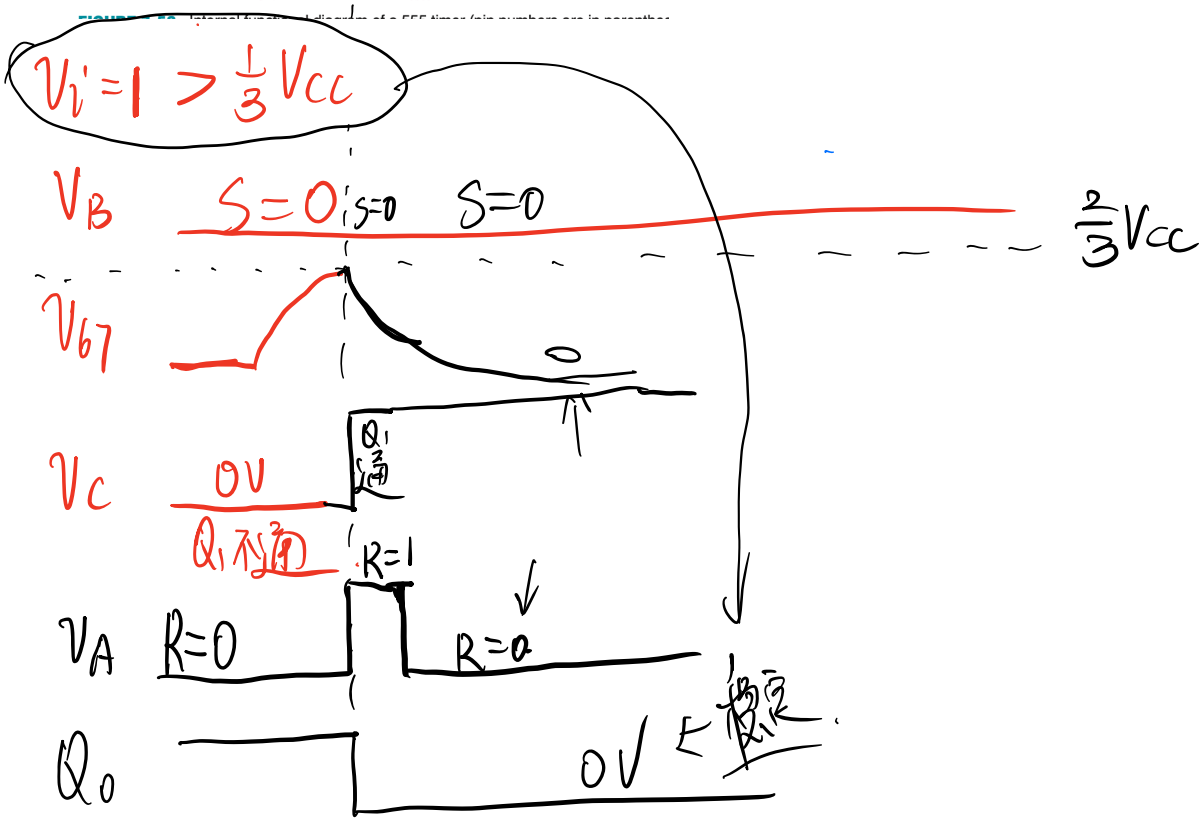
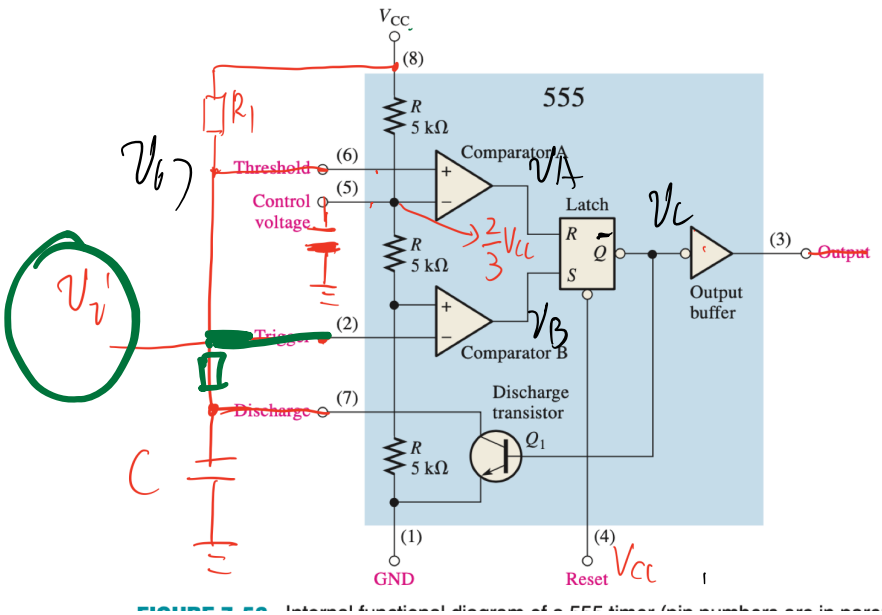


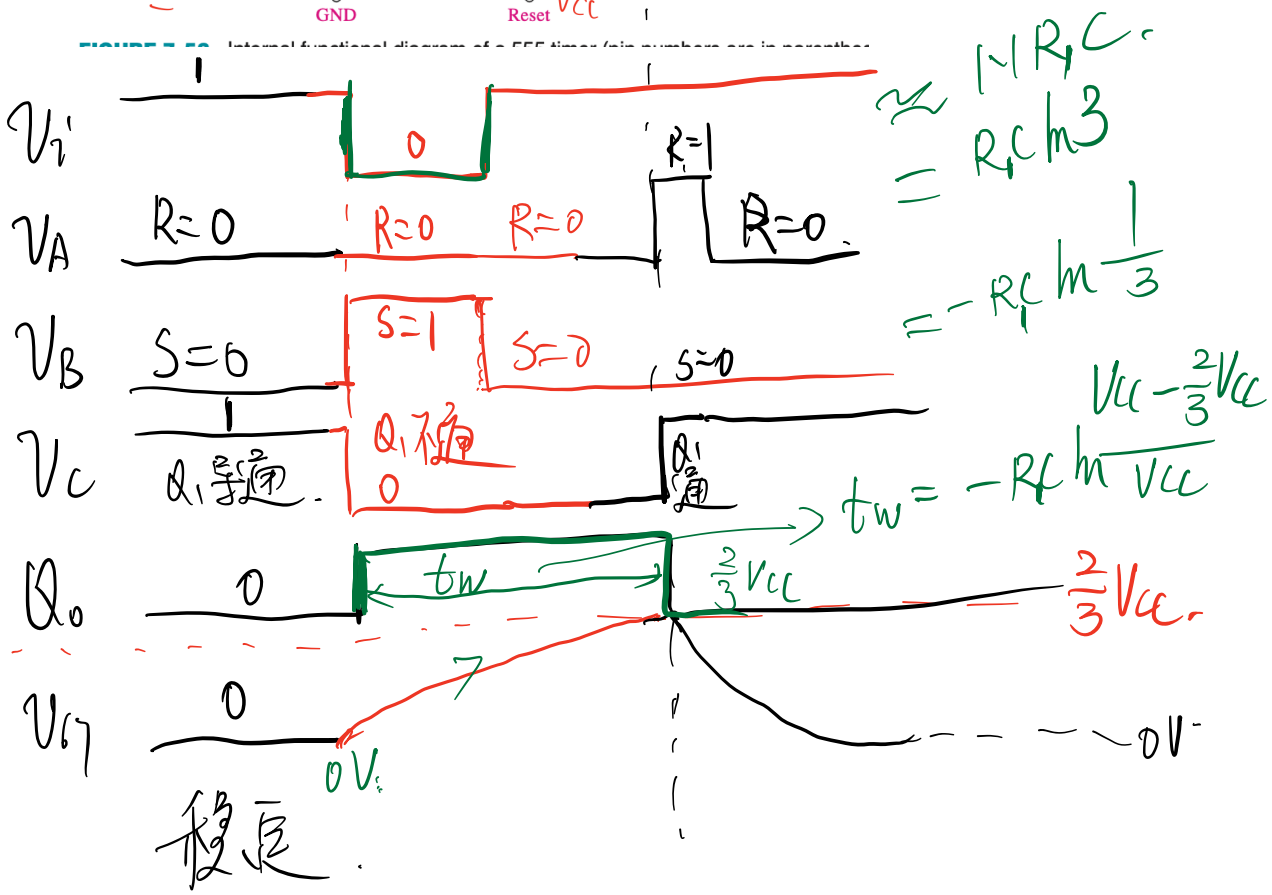
FIGURE 7–53 The 555 timer connected as a one-shot.

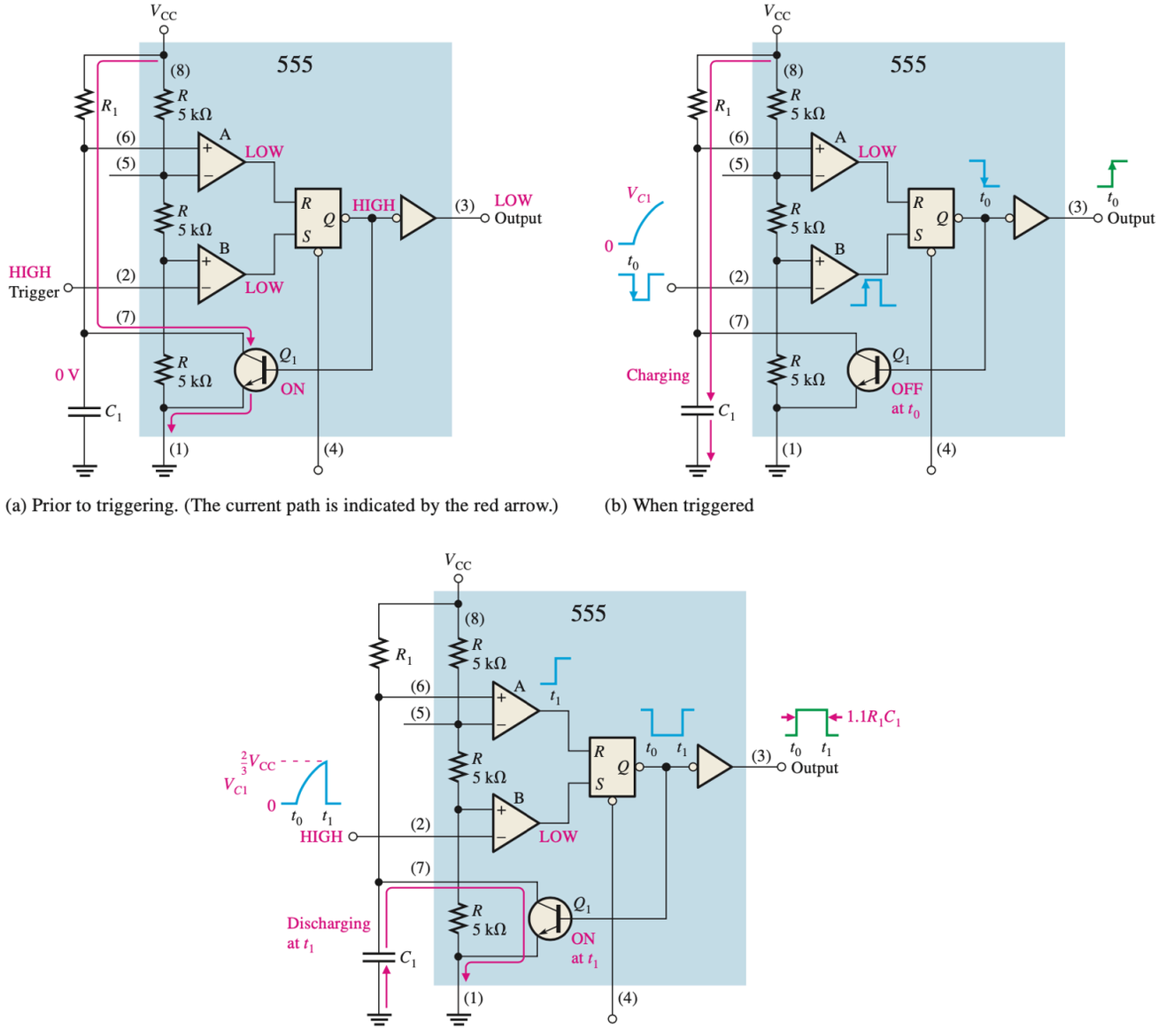
$$t_W = 1.1R_1C_1$$


V_{CC}
(8)
555
R 5 kΩ
Comparator A
Threshold
(6)
(5)
Control voltage
Latch
R
S
Q
(3)
Output
Output buffer
R 5 kΩ
(2)
Trigger
Comparator B
Discharge transistor
Q_1
(7)
Discharge
R 5 kΩ
(1)
GND
(4)
Reset
V_{CC}
V_{67}
R_1
$V_1' = 1$
C
V_A
V_B
V_C
$\frac{2}{3}V_{CC}$
$\frac{1}{3}V_{CC}$
Q_0


$V_1' = 1 > \frac{1}{3}V_{CC}$
V_B
S=0 S=0 S=0
$\frac{2}{3}V_{CC}$
V_{67}
0
V_C
0V
Q_1 飽和
Q_1 不飽和
R=1
V_A
R=0
R=0
Q_0
0V
上升沿


555
V_{CC}
(8)
R 5 kΩ
R 5 kΩ
R 5 kΩ
Threshold
(6)
Control voltage
(5)
Trigger
(2)
Discharge
(7)
Comparator A
Comparator B
Latch
Output buffer
Discharge transistor
Q_1
(3)
Output
(1)
GND
(4)
Reset
$\frac{2}{3}V_{CC}$
V_A
V_B
V_C
V_{CC}
R_1
C
V_{th}
V_i
Q_0


V_i
V_A
V_B
V_C
Q_0
V_{th}
R=0
R=1
S=1
S=0
Q_1 截止
Q_1 导通
Q_1 导通
0
t_W
$\frac{2}{3}V_{CC}$
0V
稳定
$t_W = 1.1 R_1 C$
$\approx R_1 C \ln 3$
$= -R_1 C \ln \frac{1}{3}$
$t_W = -R_1 C \ln \frac{V_{CC} - \frac{2}{3}V_{CC}}{V_{CC}}$



(a) Prior to triggering. (The current path is indicated by the red arrow.)

(b) When triggered

(c) At end of charging interval

FIGURE 7–54 One-shot operation of the 555 timer.

7–6 The Astable Multivibrator

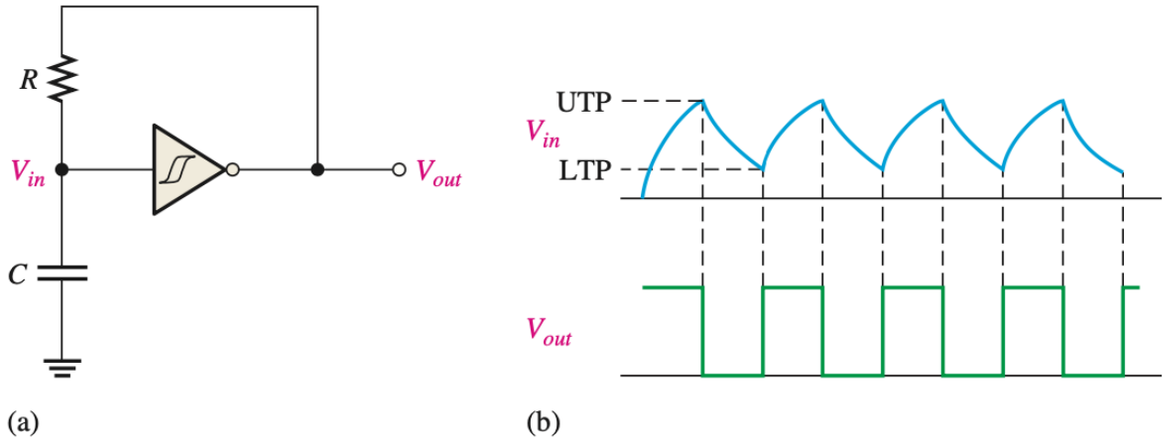


FIGURE 7–55 Basic astable multivibrator using a Schmitt trigger.

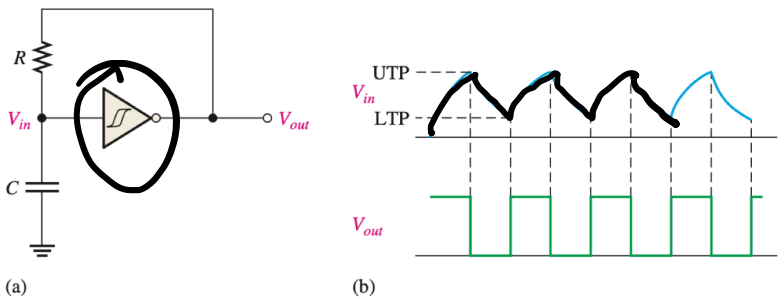


FIGURE 7–55 Basic astable multivibrator using a Schmitt trigger.

The 555 Timer as an Astable Multivibrator

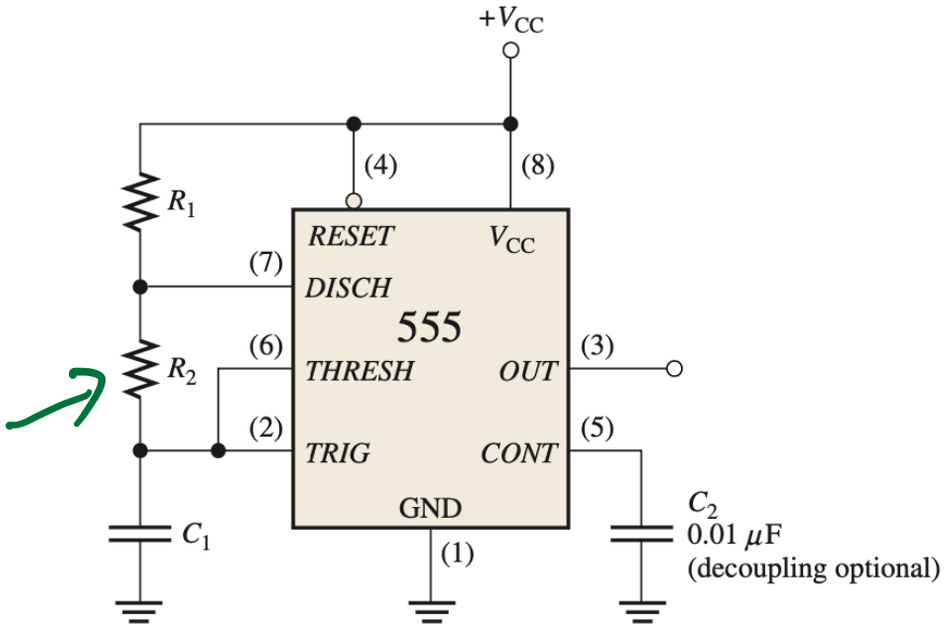


FIGURE 7–56 The 555 timer connected as an astable multivibrator (oscillator).

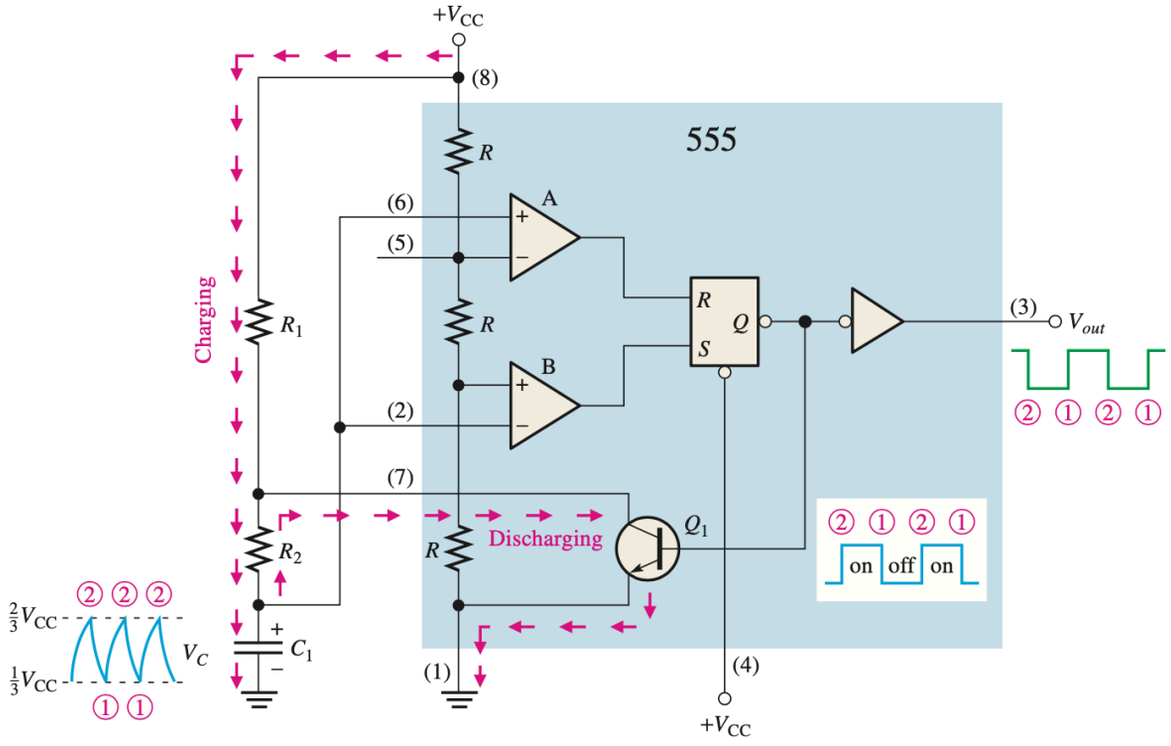
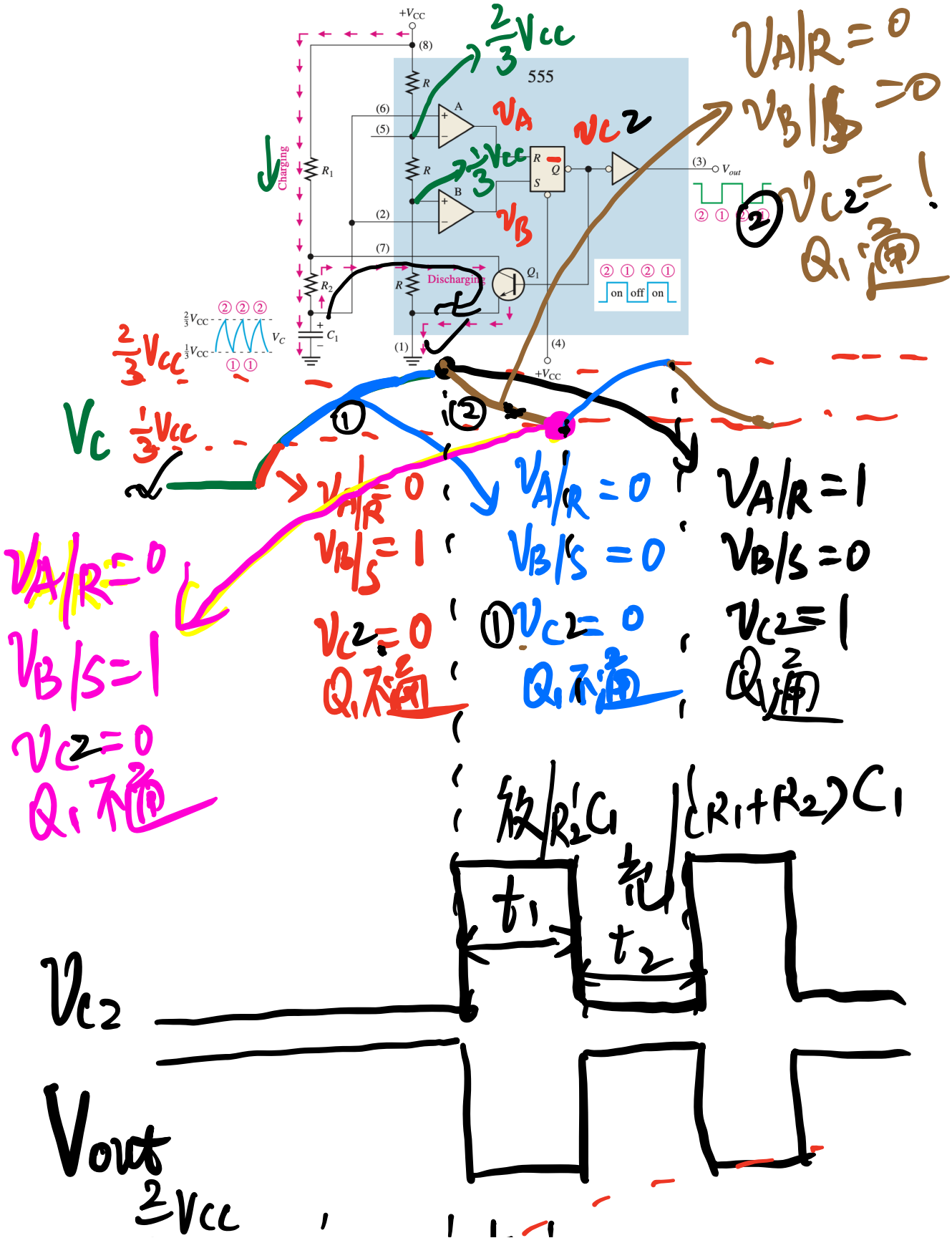


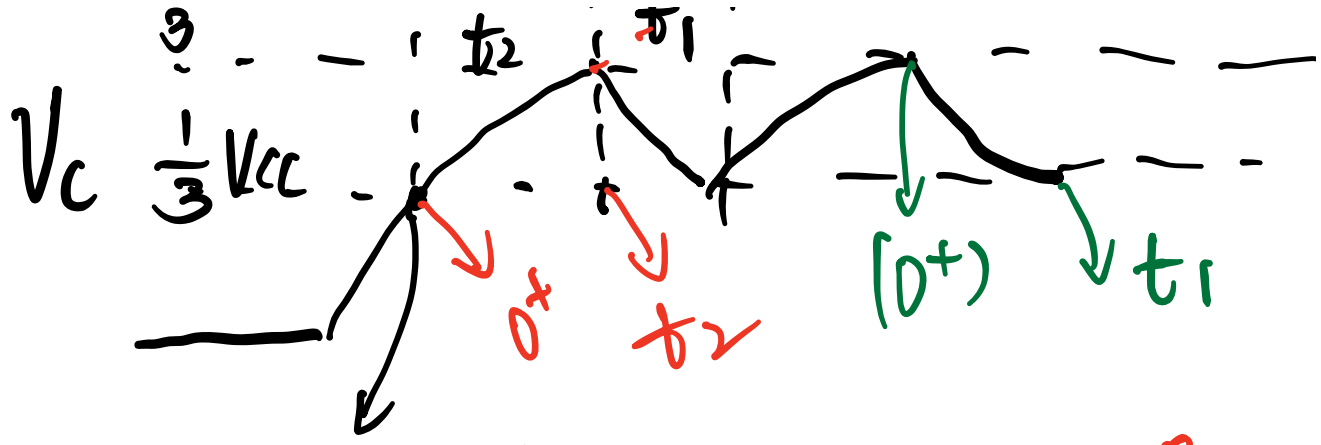
FIGURE 7–57 Operation of the 555 timer in the astable mode.

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

$$t_H = 0.7(R_1 + R_2)C_1$$

$$t_L = 0.7R_2C_1$$


555
Charging
Discharging
on off on
V_{out}
V_C
V_A
V_B
V_{C2}
$\frac{2}{3}V_{CC}$
$\frac{1}{3}V_{CC}$
$V_A/R=0$
$V_B/S=1$
$V_{C2}=0$
Q_1不通
$V_A/R=0$
$V_B/S=0$
$V_{C2}=0$
Q_1不通
$V_A/R=1$
$V_B/S=0$
$V_{C2}=1$
Q_1通
$V_A/R=0$
$V_B/S=1$
$V_{C2}=0$
Q_1不通
放 R_2C_1
充 $(R_1+R_2)C_1$
t_1
t_2
V_{C2}
V_{out}
$\frac{2}{3}V_{CC}$



t_2: $V_C(0+) = \frac{1}{3}V_{CC}$ $\quad \tau = (R_1+R_2)C_1$

$V_C(\infty) = V_{CC}$

$$V_C(t) = V_{CC} + \left(\frac{1}{3}V_{CC} - V_{CC}\right)e^{-\frac{t}{(R_1+R_2)C_1}}$$

$$= V_{CC} - \frac{2}{3}V_{CC}\, e^{-\frac{t}{(R_1+R_2)C_1}}$$

$$V_C(t_2) = \frac{2}{3}V_{CC}$$

$$= V_{CC} - \frac{2}{3}V_{CC}\, e^{-\frac{t_2}{(R_1+R_2)C_1}}$$

$$\Rightarrow \frac{1}{3} = \frac{2}{3}e^{-\frac{t_2}{(R_1+R_2)C_1}}$$

$$\Rightarrow \ln\frac{1}{2} = -\frac{t_2}{(R_1+R_2)C_1}$$

$$t_2 = \ln 2 (R_1 + R_2) C_1$$

t_1: $V_c(0+) = \frac{2}{3}V_{cc}$ $\quad V_c(\infty) = 0$

$V_c(t_1) = \frac{1}{3}V_{cc}$ $\quad \tau = R_2 C_1$

$$V_c(t) = 0 + \left[\frac{2}{3}V_{cc} - 0\right] e^{-\frac{t}{R_2 C_1}}$$

$$V_c(t_1) = \frac{1}{3}V_{cc}$$

$$= \frac{2}{3}V_{cc} e^{-\frac{t_1}{R_2 C_1}}$$

$$\Rightarrow \ln \frac{1}{2} = -\frac{t_1}{R_2 C_1}$$

$$\Rightarrow t_1 = R_2 C_1 \ln 2$$

$t_1 = R_2 C_1 \ln 2$ $\quad$ $t_2 = (R_1 + R_2) C_1 \ln 2$

$\Rightarrow T = t_1 + t_2$

$= (R_1 + 2R_2) C_1 \ln 2$

$$Duty\ cycle = \frac{t_H}{T}$$

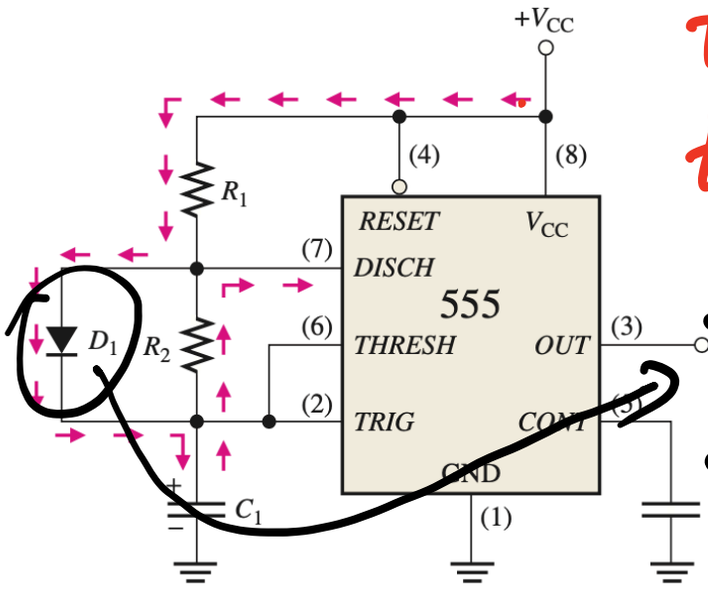
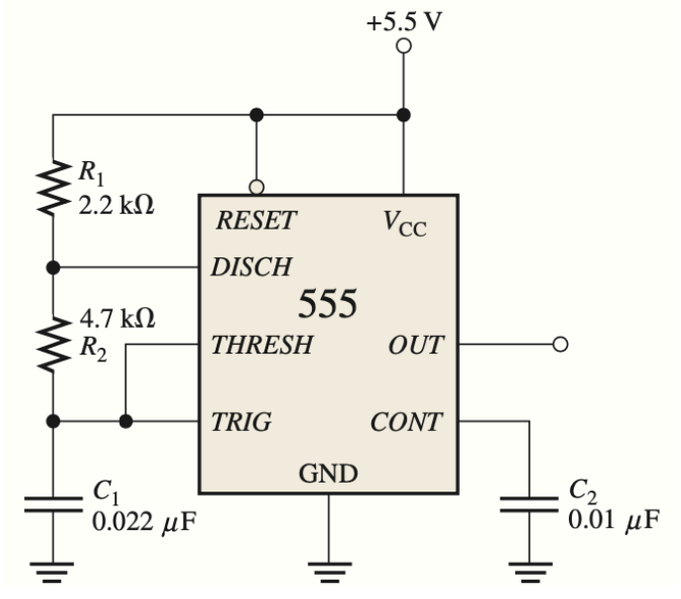


FIGURE 7–58 The addition of diode D_1 allows the duty cycle of the output to be adjusted to less than 50 percent by making $R_1 < R_2$.

EXAMPLE 7–14

A 555 timer configured to run in the astable mode (pulse oscillator) is shown in Figure 7–60. Determine the frequency of the output and the duty cycle.



MultiSim

FIGURE 7–60 Open file F07-60 to verify operation.