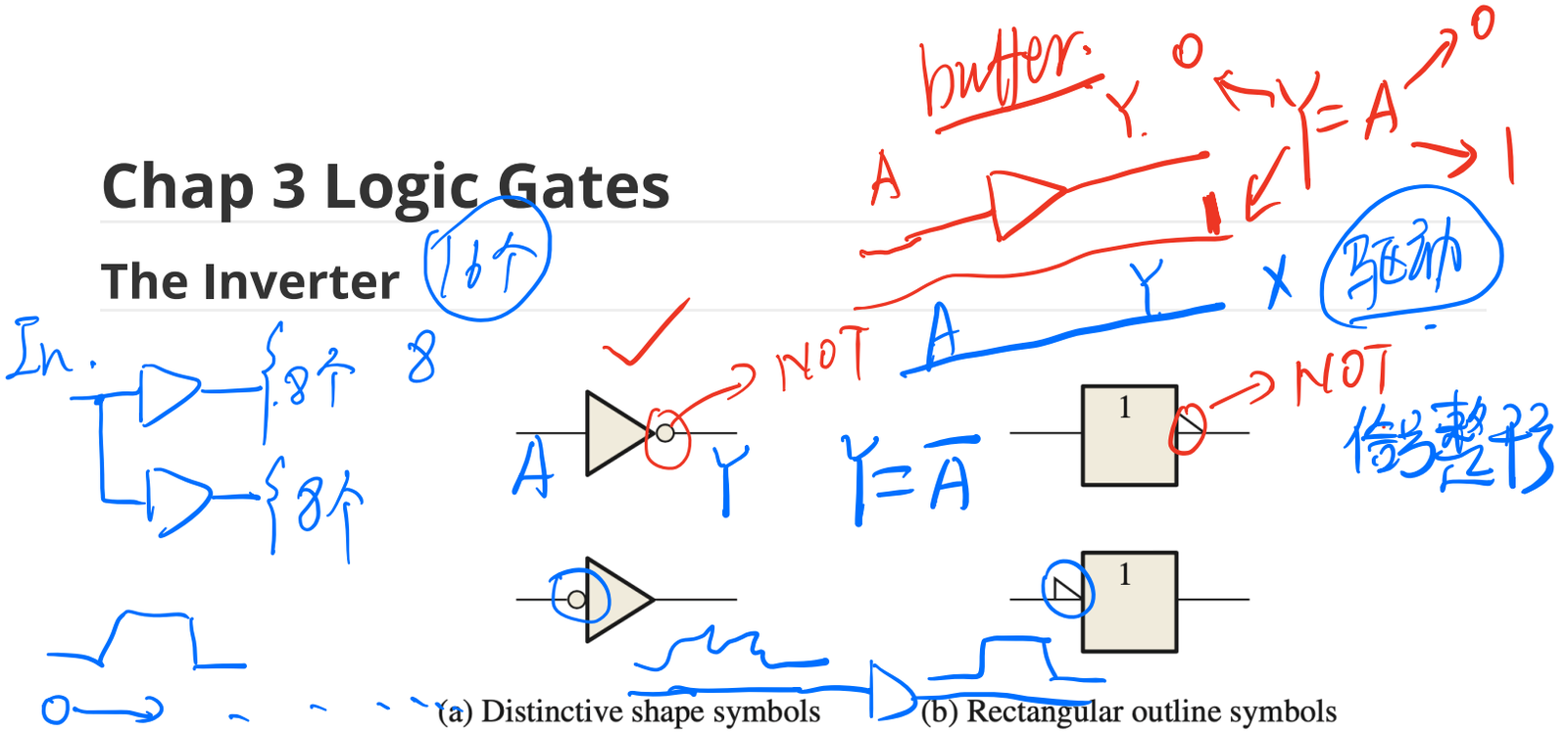
Chap 3 Logic Gates

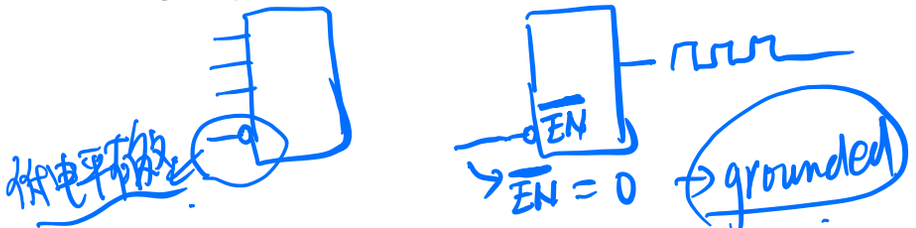
The Inverter



(a) Distinctive shape symbols with negation indicators

(b) Rectangular outline symbols with polarity indicators

FIGURE 3–1 Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984/ Std. 91a-1991).



The polarity or level indicator is a "triangle" ( ) that indicates inversion when it appears on the input or output of a logic element, as shown in Figure 3–1(b). When appear- ing on the input, it means that a LOW level is the active or asserted input state. When appearing on the output, it means that a LOW level is the active or asserted output state.

EXAMPLE 3–1

A waveform is applied to an inverter in Figure 3–4. Determine the output waveform corresponding to the input and show the timing diagram. According to the placement of the bubble, what is the active output state?

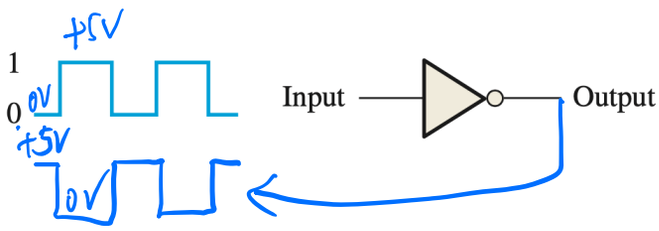


FIGURE 3–4

Logic Expression for an Inverter

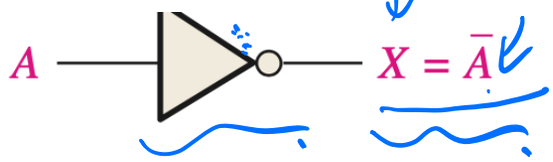
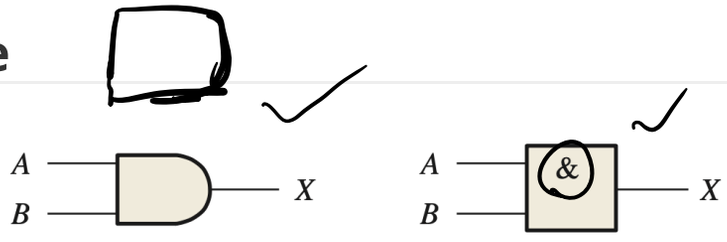


FIGURE 3–6 The inverter complements an input variable.

A	X
0	1
1	0

The AND Gate



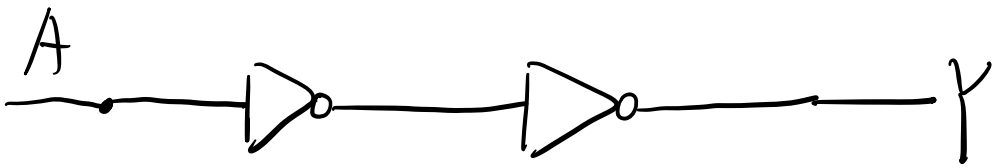
(a) Distinctive shape

(b) Rectangular outline with the AND (&) qualifying symbol

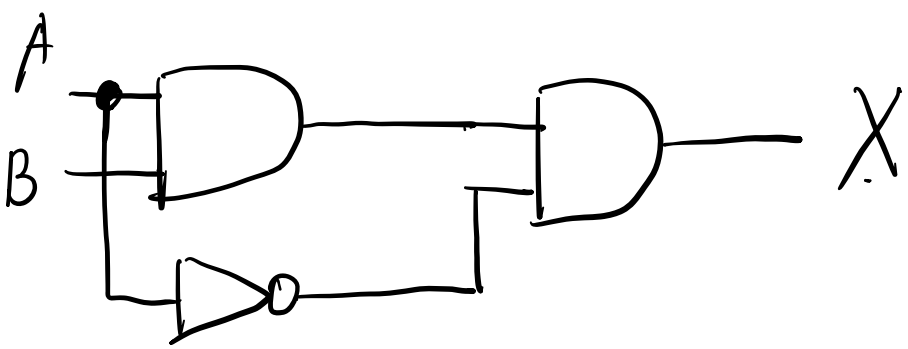
FIGURE 3–8 Standard logic symbols for the AND gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

$X = AB$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1



$$Y = \overline{\overline{A}} = A$$



$$X = (A\,B)\,\bar{A}$$

0 → 0

1

A	B	X	X
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	0

For an AND gate, all HIGH inputs produce a HIGH output.

TABLE 3–2

Truth table for a 2-input AND gate.

Inputs		Output
A	***B***	***X***
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

EXAMPLE 3–2

TABLE 3–3

Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

EXAMPLE 3–4

For the two input waveforms, *A* and *B*, in Figure 3–12, show the output waveform with its proper relation to the inputs.

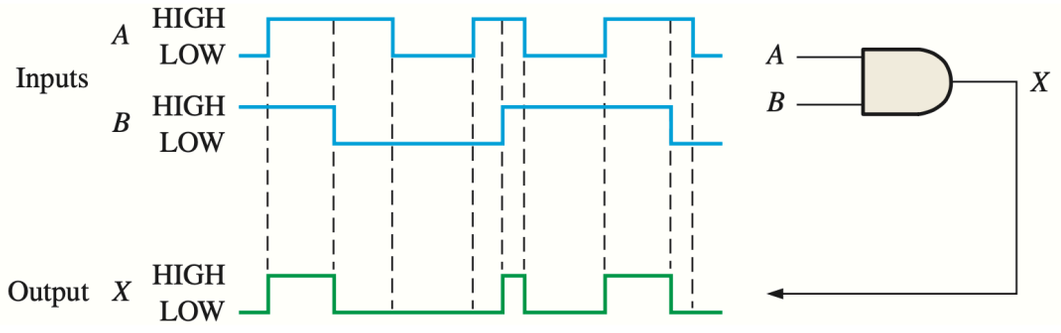
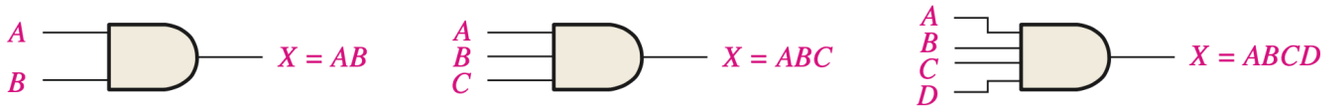


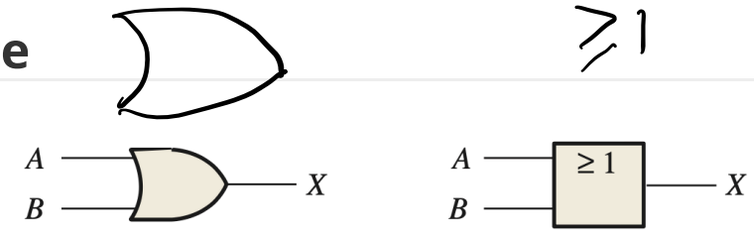
FIGURE 3–12



(a) (b) (c)

FIGURE 3–15 Boolean expressions for AND gates with two, three, and four inputs.

The OR Gate



(a) Distinctive shape

(b) Rectangular outline with the OR (≥ 1) qualifying symbol

FIGURE 3–18 Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

$X = A + B$

TABLE 3–5

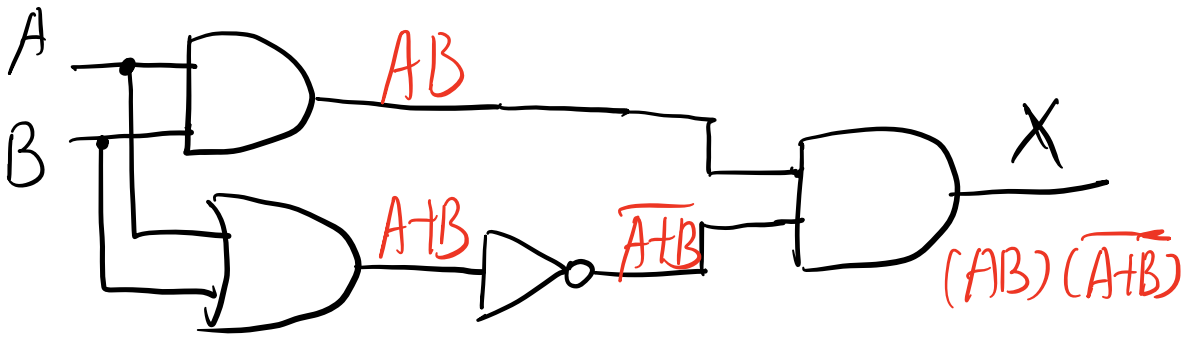
Truth table for a 2-input OR gate.

Inputs		Output
A	**B**	**X**
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

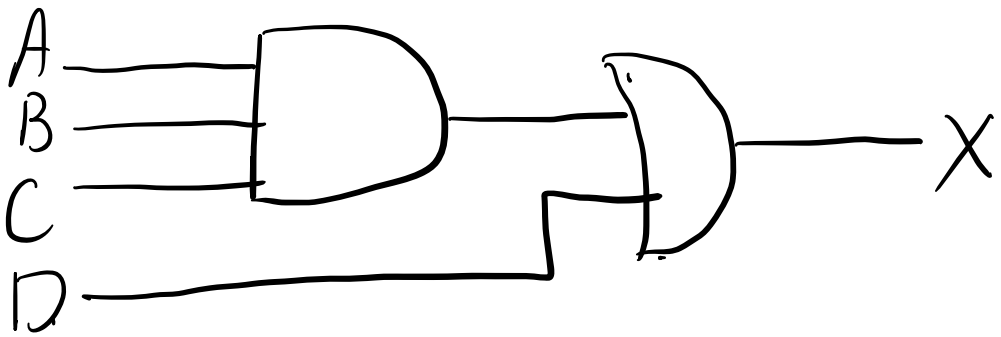
OR. AND NOT. Logic complete set.

NAND



$$X = (AB)\ \overline{(A+B)}$$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	0



$X = \overline{ABC} + \overline{D}$

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0 1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0

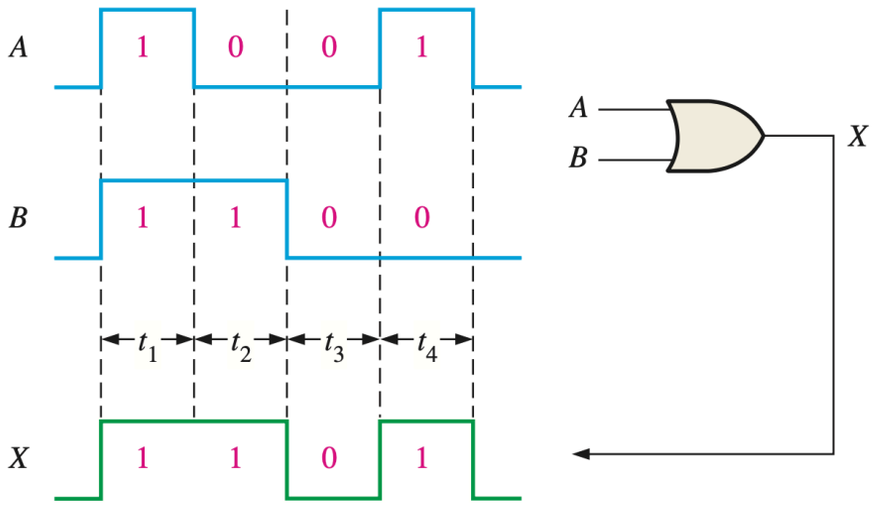


FIGURE 3–20 Example of OR gate operation with a timing diagram showing input and output time relationships.

EXAMPLE 3–9

For the 3-input OR gate in Figure 3–23, determine the output waveform in proper time relation to the inputs.

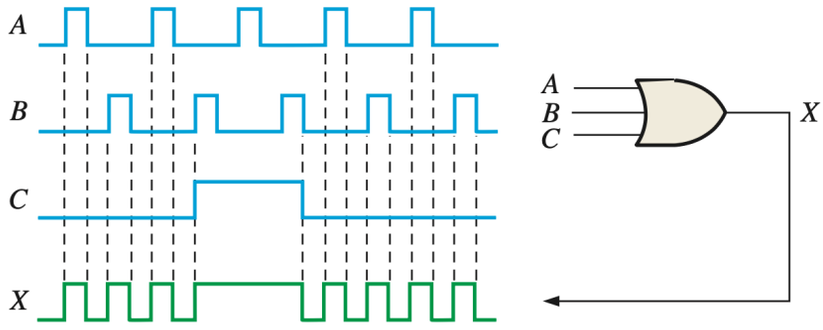
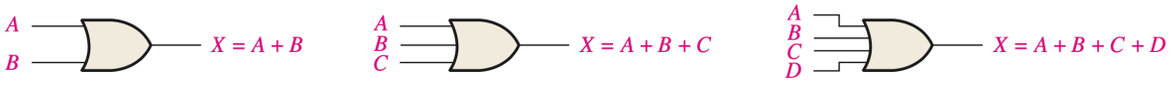


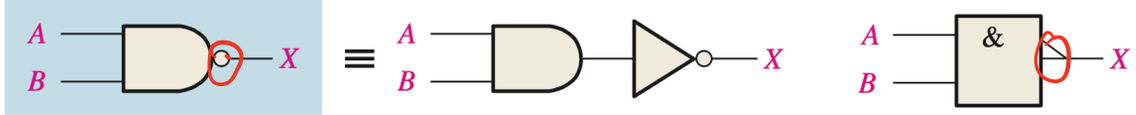
FIGURE 3–23



(a) (b) (c)

FIGURE 3–24 Boolean expressions for OR gates with two, three, and four inputs.

The NAND Gate



(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent

(b) Rectangular outline, 2-input NAND gate with polarity indicator

FIGURE 3–26 Standard NAND gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

$X = \overline{AB}$

TABLE 3–7

Truth table for a 2-input NAND gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

1 = HIGH, 0 = LOW.

EXAMPLE 3–11

Show the output waveform for the 3-input NAND gate in Figure 3–29 with its proper time relationship to the inputs.

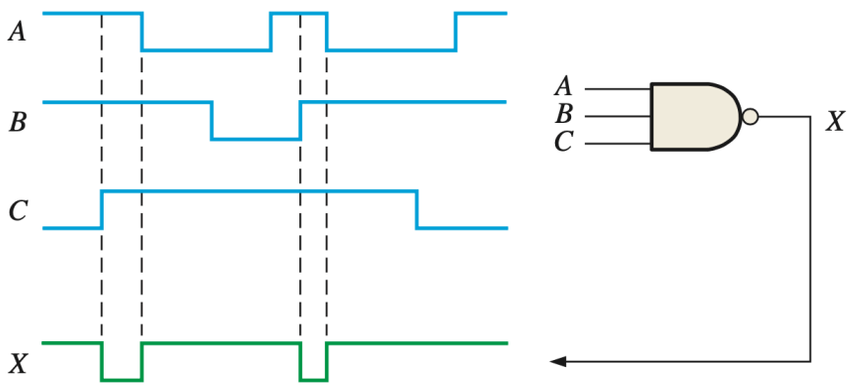
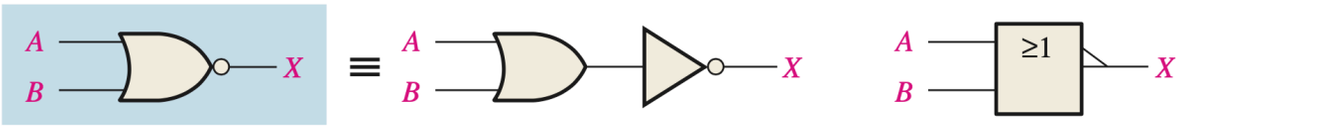


FIGURE 3–29

The NOR Gate

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

$X = \overline{A+B}$



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent

(b) Rectangular outline, 2-input NOR gate with polarity indicator

FIGURE 3–34 Standard NOR gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

EXAMPLE 3–16

Show the output waveform for the 3-input NOR gate in Figure 3–37 with the proper time relation to the inputs.

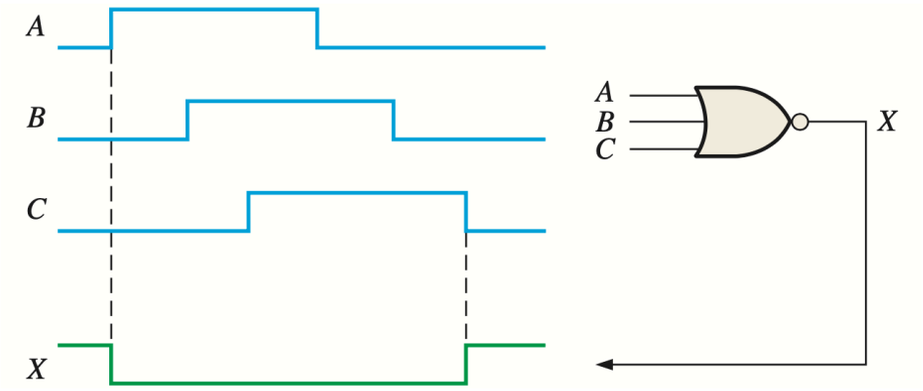


FIGURE 3–37

The Exclusive-OR and Exclusive-NOR Gates

(a) Distinctive shape

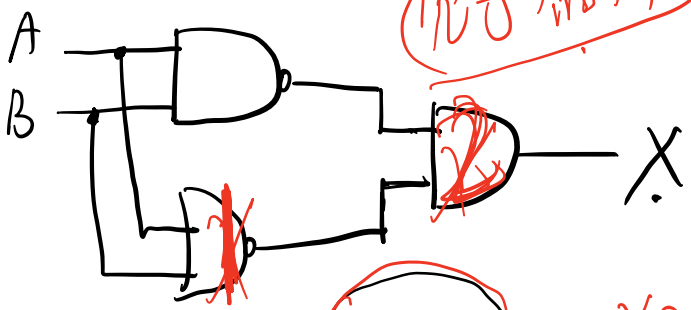
(b) Rectangular outline

FIGURE 3–42 Standard logic symbols for the exclusive-OR gate.

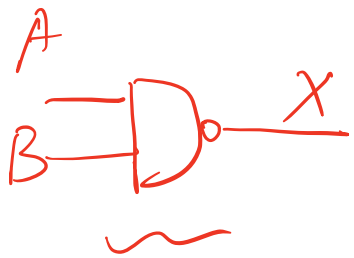
(a) Distinctive shape

(b) Rectangular outline

FIGURE 3–45 Standard logic symbols for the exclusive-NOR gate.



冗余器件



$X = \overline{(AB)}\ \overline{(A+B)}$

$X = \overline{AB}$

$X = \overline{AB}$

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

IC

~~设计~~

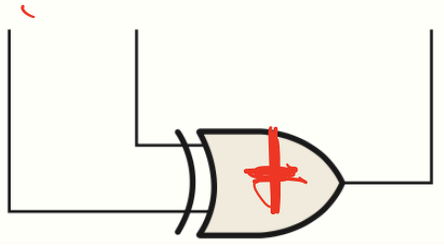
EDA

Synopsys Cadence.

TABLE 3–13

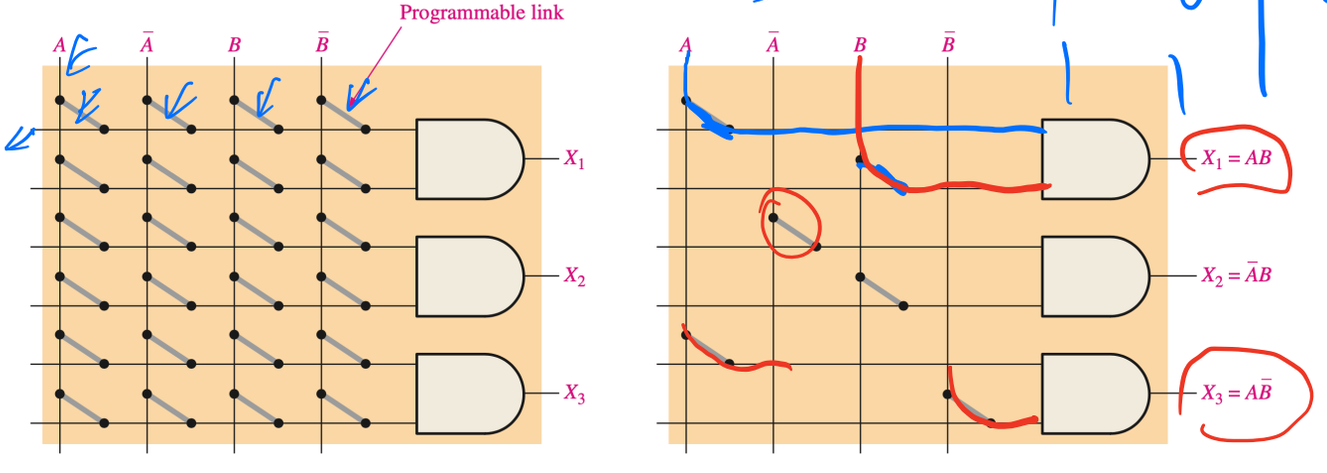
An XOR gate used to add two bits.

Input Bits		Output (Sum)
A	*B*	Σ
0	0	0
0	1	1
1	0	1
1	1	0 (without the 1 carry bit)



Programmable Logic

The AND Array + OR Array

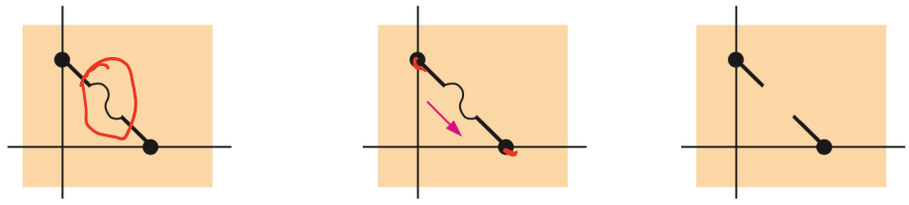


(a) Unprogrammed (b) Programmed

FIGURE 3–49 Concept of a programmable AND array.

Programmable Link Process Technologies

Fuse Technology



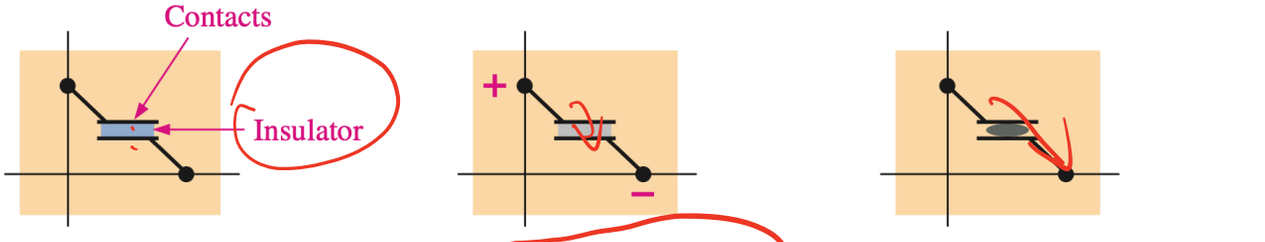
(a) Fuse intact before programming

(b) Programming current

(c) Fuse open after programming

FIGURE 3–51 The programmable fuse link.

Antifuse Technology



(a) Antifuse is open before programming.

(b) Programming voltage breaks down insulation layer to create contact.

(c) Antifuse is effectively shorted after programming.

FIGURE 3–52 The programmable antifuse link.

EPROM Technology

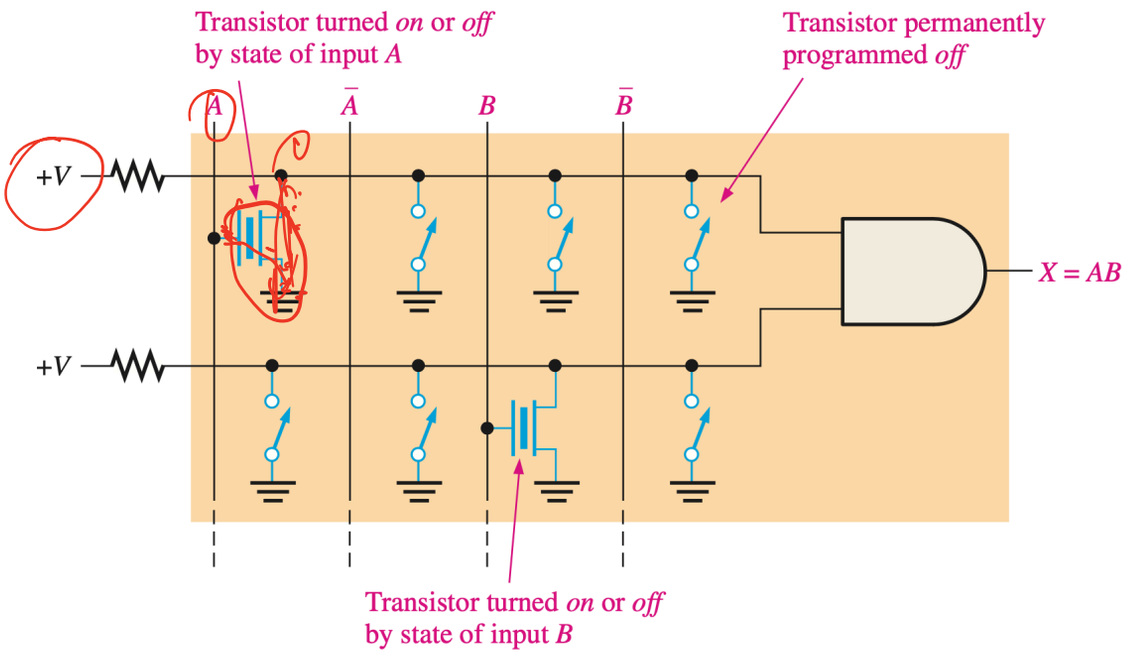
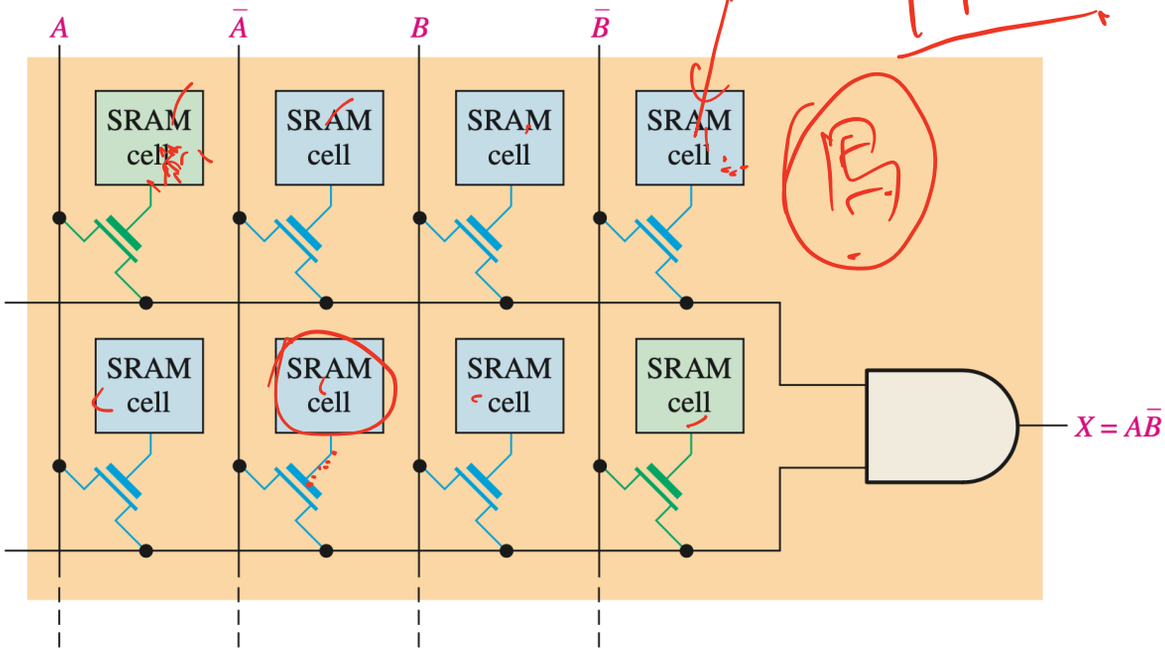


FIGURE 3–53 A simple AND array with EPROM technology. Only one gate in the array is shown for simplicity.

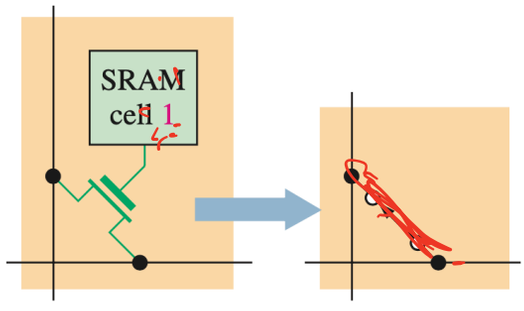
Flash Technology

Flash technology is based on a single transistor link and is both nonvolatile and reprogram- mable. Flash elements are a type of EEPROM but are faster and result in higher density devices than the standard EEPROM link. A detailed discussion of the flash memory element can be found in Chapter 11.

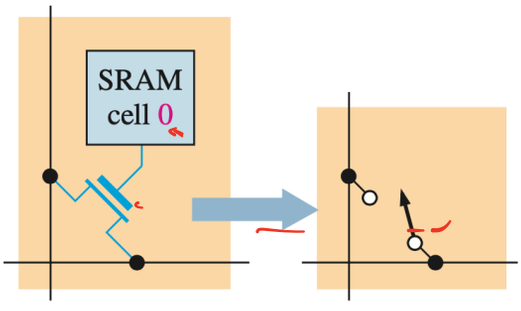
SRAM Technology



(a) SRAM-based programmable array



(b) Transistor *on*



(c) Transistor *off*

FIGURE 3–54 Concept of an AND array with SRAM technology.

IC.

TABLE 3–14

74 series logic families based on circuit technology.

Circuit Type	Description	Circuit Technology
ABT	Advanced BiCMOS	BiCMOS
AC	Advanced CMOS	CMOS
ACT	Bipolar compatible AC	CMOS
AHC	Advanced high-speed CMOS	CMOS
AHCT	Bipolar compatible AHC	CMOS
ALB	Advanced low-voltage BiCMOS	BiCMOS
ALS	Advanced low-power Schottky	Bipolar
ALVC	Advanced low-voltage CMOS	CMOS
AUC	Advanced ultra-low-voltage CMOS	CMOS
AUP	Advanced ultra-low-power CMOS	CMOS
AS	Advanced Schottky	Bipolar
AVC	Advanced very-low-power CMOS	CMOS
BCT	Standard BiCMOS	BiCMOS
F	Fast	Bipolar
FCT	Fast CMOS technology	CMOS
HC	High-speed CMOS	CMOS
HCT	Bipolar compatible HC	CMOS
LS	Low-power Schottky	Bipolar
LV-A	Low-voltage CMOS	CMOS
LV-AT	Bipolar compatible LV-A	CMOS
LVC	Low-voltage CMOS	CMOS
LVT	Low-voltage biCMOS	BiCMOS
S	Schottky	Bipolar

Propagation Delay Time

EXAMPLE 3–23

Show the propagation delay times of an inverter.

Solution

An input/output pulse of an inverter is shown in Figure 3–67, and the propagation delay times, t_{PHL} and t_{PLH}, are indicated. In this case, the delays are measured between the 50% points of the corresponding edges of the input and output pulses. The values of t_{PHL} and t_{PLH} are not necessarily equal but in many cases they are the same.

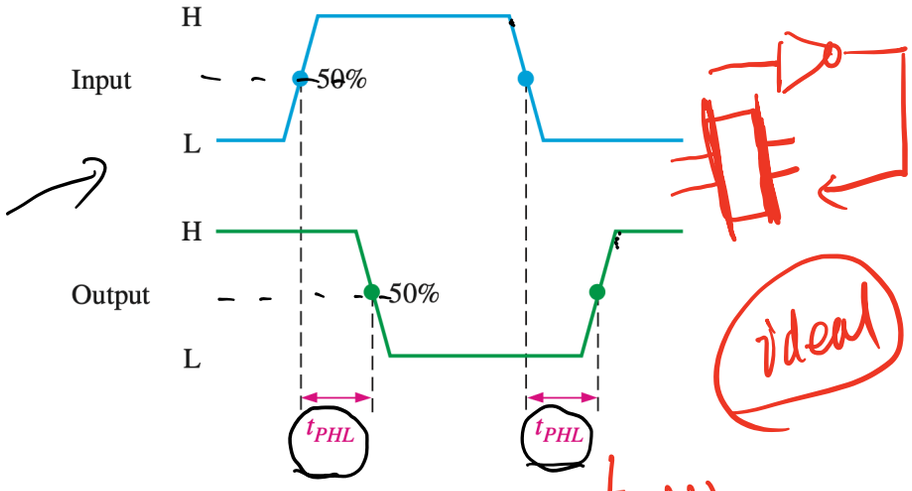


FIGURE 3–67

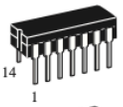
datasheets

Quad 2-Input NAND Gate High-Performance Silicon–Gate CMOS

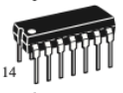
The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates

MC54/74HC00A



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

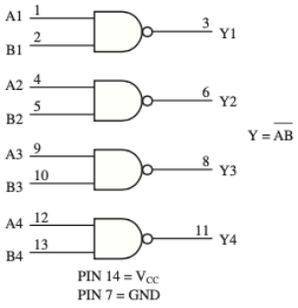
D SUFFIX
SOIC PACKAGE
CASE 751A-03

DT SUFFIX
TSSOP PACKAGE
CASE 948G-01

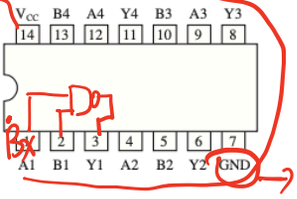
ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

LOGIC DIAGRAM



Pinout: 14–Load Packages (Top View)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	−65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	Plastic DIP, SOIC or TSSOP Package	260	
	Ceramic DIP	300	

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125° C
Ceramic DIP: – 10 mW/°C from 100° to 125° C
SOIC Package: – 7 mW/°C from 65° to 125° C
TSSOP Package: – 6.1 mW/°C from 65° to 125° C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		in	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC CHARACTERISTICS (Voltages Referenced to GND) MC54/74HC00A

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V, $\|I_{out}\| \le 20\mu A$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V, $\|I_{out}\| \le 20\mu A$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL}, $\|I_{out}\| \le 20\mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL}, $\|I_{out}\| \le 2.4mA$	3.0	2.48	2.34	2.20	
		$\|I_{out}\| \le 4.0mA$	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 5.2mA$	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL}, $\|I_{out}\| \le 20\mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL}, $\|I_{out}\| \le 2.4mA$	3.0	0.26	0.33	0.40	
		$\|I_{out}\| \le 4.0mA$	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2mA$	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND, I_{out} = 0μA	6.0	1.0	10	40	μA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)	22	pF

FIGURE 3–65 CMOS logic. Partial data sheet for a 54/74HC00A quad 2-input NAND gate. The 54 prefix indicates military grade and the 74 prefix indicates commercial grade.

DC Supply Voltage

The typical dc supply voltage for CMOS logic is either 5 V, 3.3 V, 2.5 V, or 1.8 V, depend- ing on the category. An advantage of CMOS is that the supply voltages can vary over a wider range than for bipolar logic. The 5 V CMOS can tolerate supply variations from 2 V to 6 V and still operate properly although propagation delay time and power dissipation are significantly affected. The 3.3 V CMOS can operate with supply voltages from 2 V to 3.6 V. The typical dc supply voltage for bipolar logic is 5.0 V with a minimum of 4.5 V and a maximum of 5.5 V.

Power Dissipation

$$P_D = V_{CC}\left(\frac{I_{CCH} + I_{CCL}}{2}\right)$$

The HC family, for example, has a power of 2.75 mW/gate at 0 Hz (quiescent) and 600 mW/gate at 1 MHz.

Input and Output Logic Levels

*V*IL is the LOW level input voltage for a logic gate, and *V*IH is the HIGH level input volt- age. The 5 V CMOS accepts a maximum voltage of 1.5 V as *V*IL and a minimum voltage of 3.5 V as *V*IH. Bipolar logic accepts a maximum voltage of 0.8 V as *V*IL and a minimum voltage of 2 V as *V*IH.

*V*OL is the LOW level output voltage and *V*OH is the HIGH level output voltage. For 5 V CMOS, the maximum *V*OL is 0.33 V and the minimum *V*OH is 4.4 V. For bipolar logic, the maximum *V*OL is 0.4 V and the minimum *V*OH is 2.4 V. All values depend on operating conditions as specified on the data sheet.

Speed-Power Product (SPP)

$$SPP = t_p P_D$$

This parameter (**speed-power product**) can be used as a measure of the performance of a logic circuit taking into account the propagation delay time and the power dissipation.

EXAMPLE 3–24

A certain gate has a propagation delay of 5 ns and $I_{CCH} = 1$ mA and $I_{CCL} = 2.5$ mA with a dc supply voltage of 5 V. Determine the speed-power product.

Solution

$$P_D = V_{CC}\left(\frac{I_{CCH} + I_{CCL}}{2}\right) = 5\text{ V}\left(\frac{1\text{ mA} + 2.5\text{ mA}}{2}\right) = 5\text{ V}(1.75\text{ mA}) = 8.75\text{ mW}$$

$$SPP = (5\text{ ns})\,(8.75\text{ mW}) = \mathbf{43.75\ pJ}$$

Fan-Out and Loading

$$\text{Unit loads} = \frac{I_{OL}}{I_{IL}} = \frac{8.0\text{ mA}}{0.4\text{ mA}} = 20$$

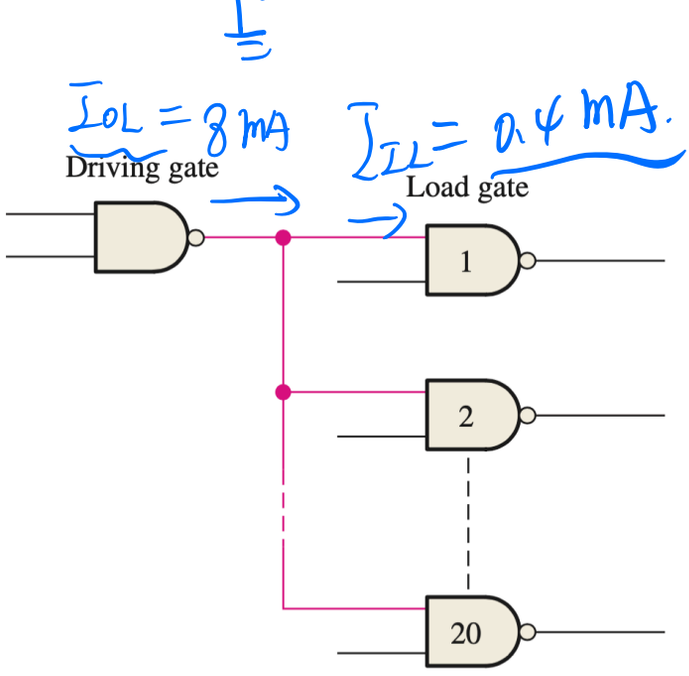
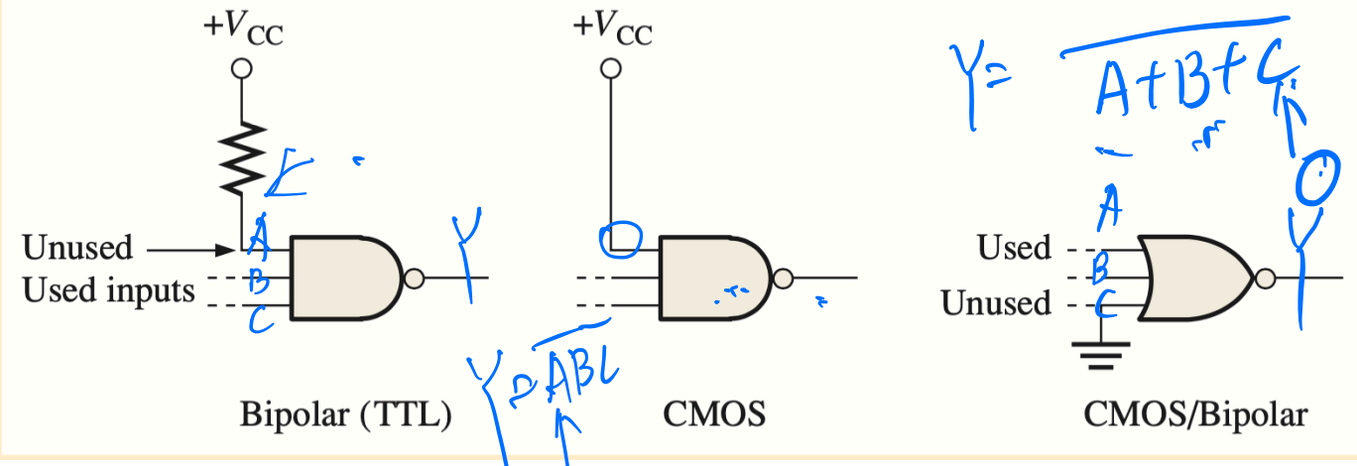
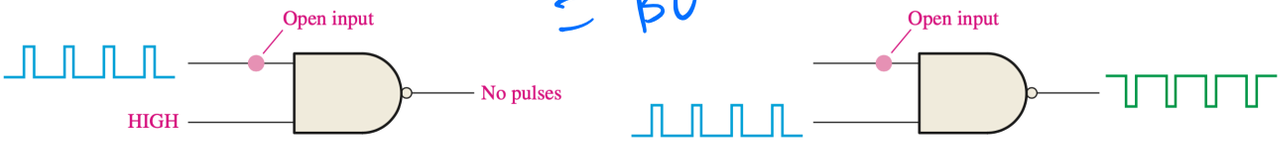


FIGURE 3–68 The LS family NAND gate output fans out to a maximum of 20 LS family gate inputs.

Unused inputs



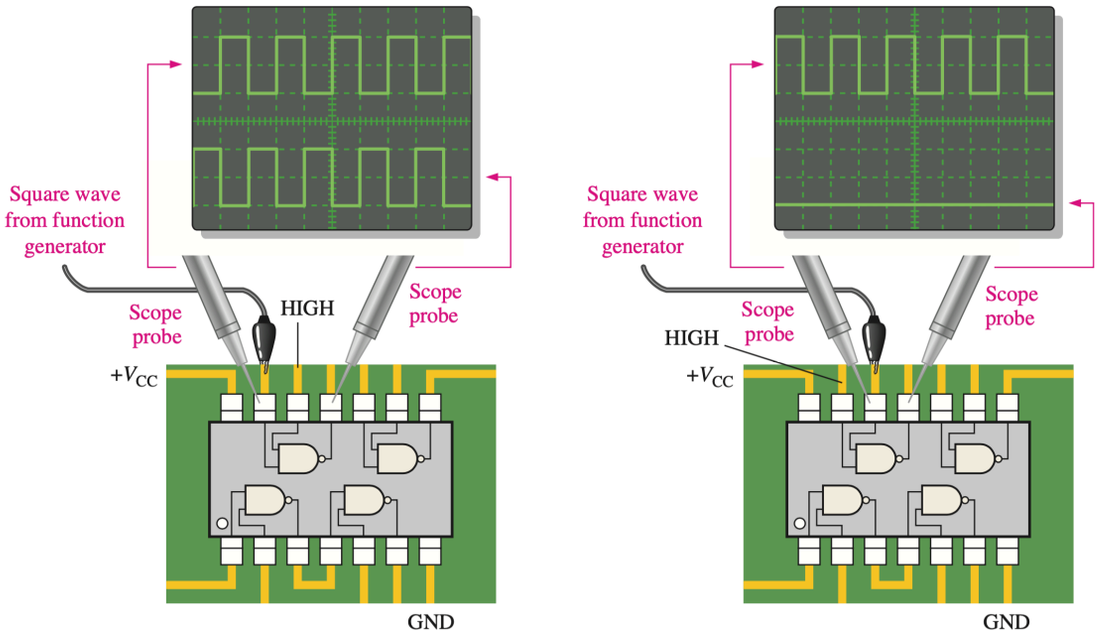
Troubleshooting



(a) Application of pulses to the open input will produce no pulses on the output.

(b) Application of pulses to the good input will produce output pulses for bipolar NAND and AND gates because an open input typically acts as a HIGH. It is uncertain for CMOS.

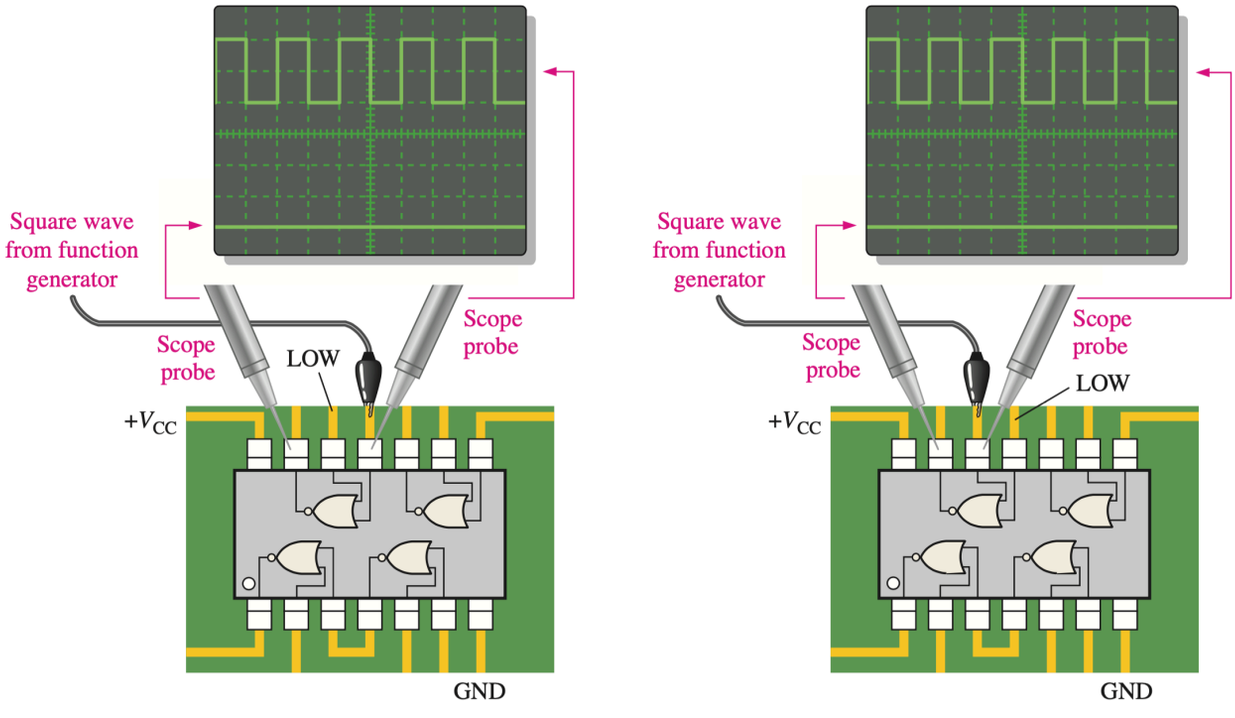
FIGURE 3–69 The effect of an open input on a NAND gate.



(a) Pin 13 input and pin 11 output OK

(b) Pin 12 input is open.

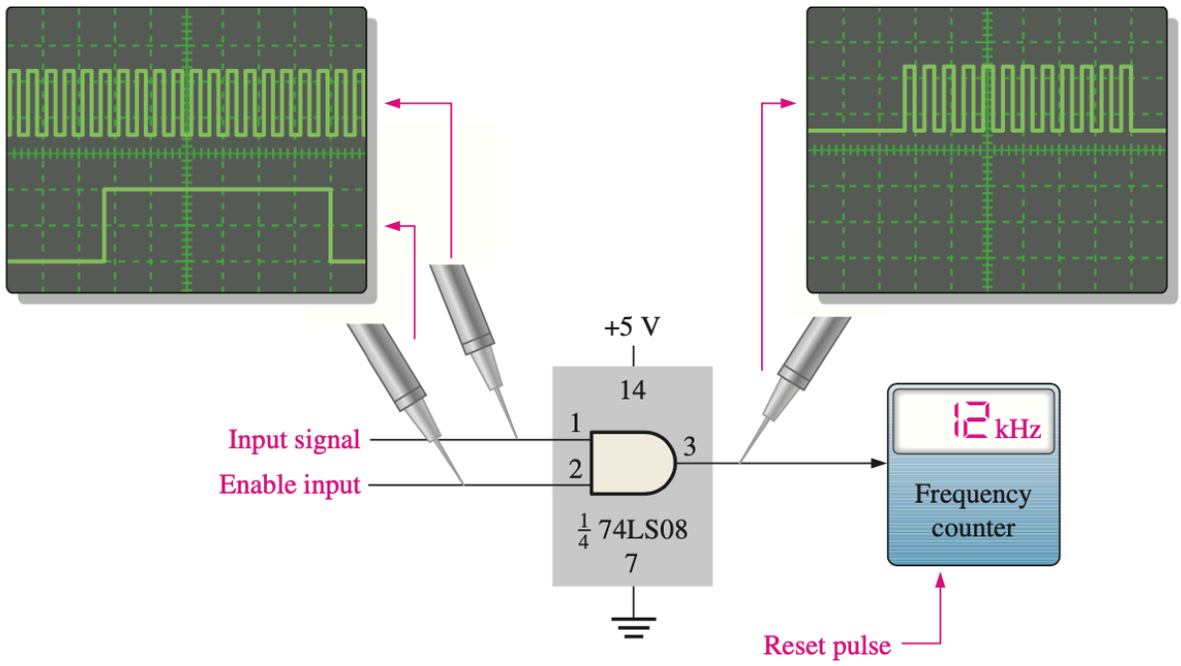
FIGURE 3–70 Troubleshooting a NAND gate for an open input.



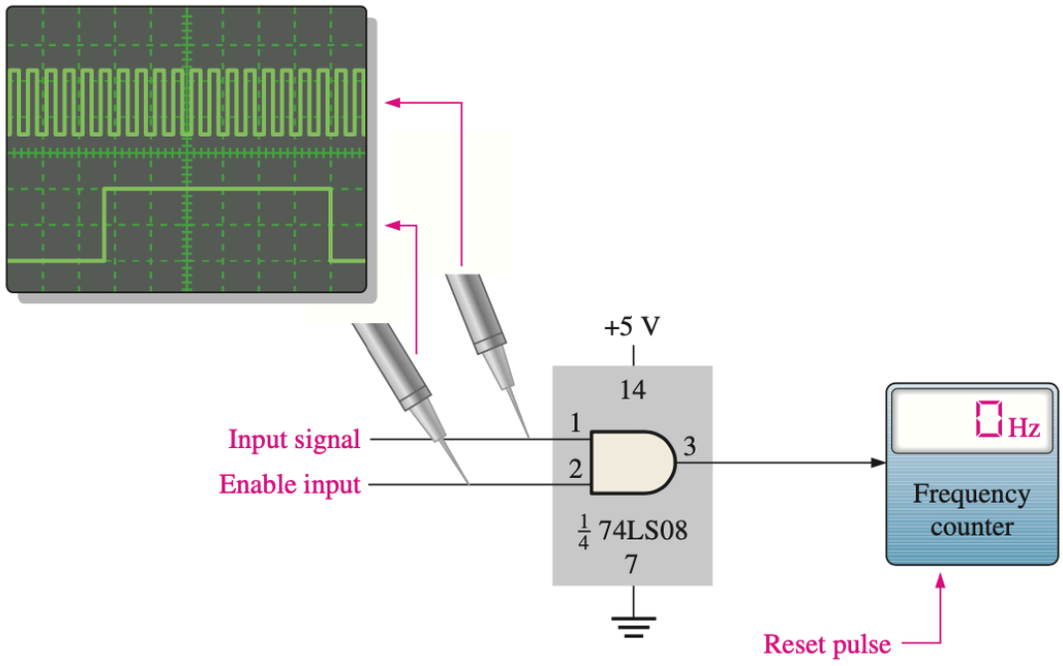
(a) Pulse input on pin 11. No pulse output.

(b) Pulse input on pin 12. No pulse output.

FIGURE 3–71 Troubleshooting a NOR gate for an open output.

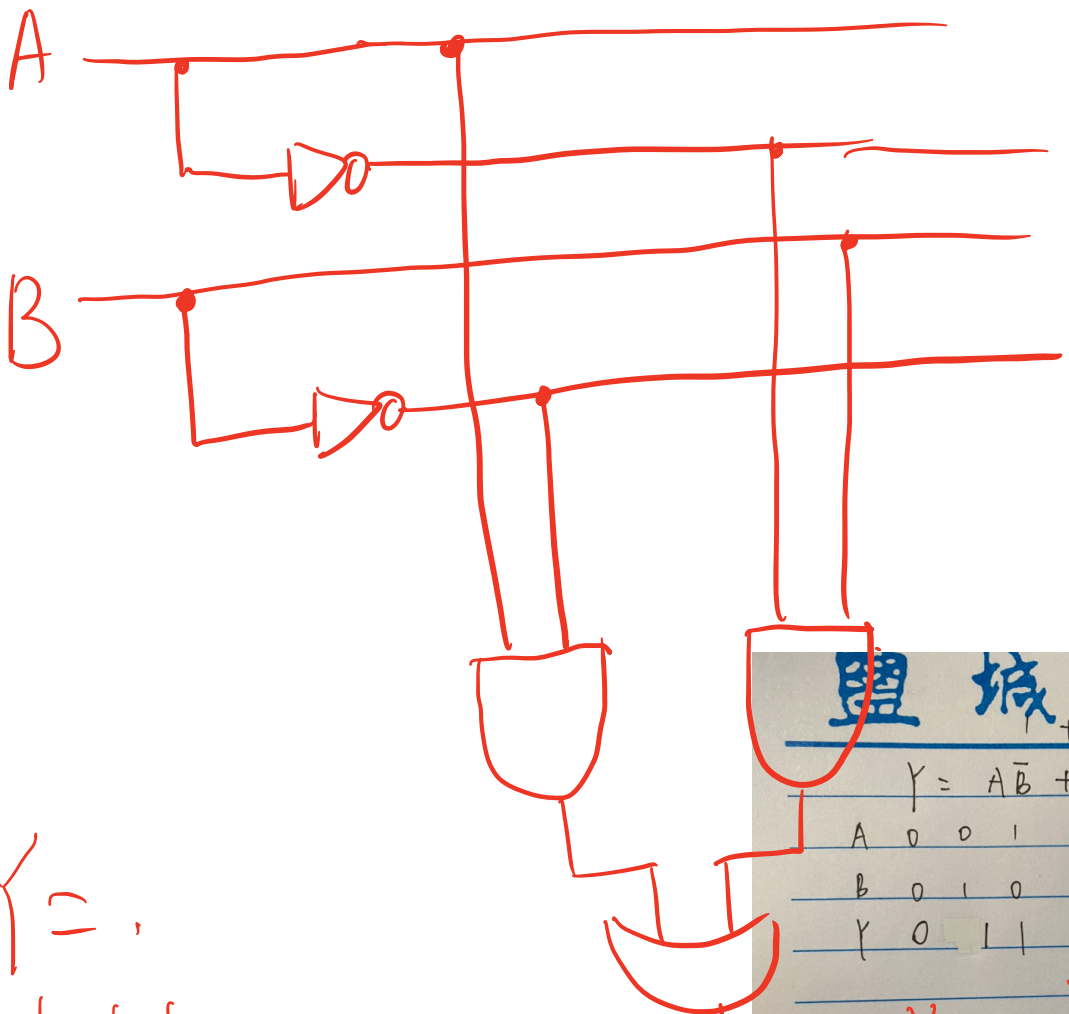


(a) The counter is working properly.



(b) The counter is not measuring a frequency.

FIGURE 3–73



Y=.

真值表.

描述一下逻辑功能.