Shift Registers

Shift Register Operations

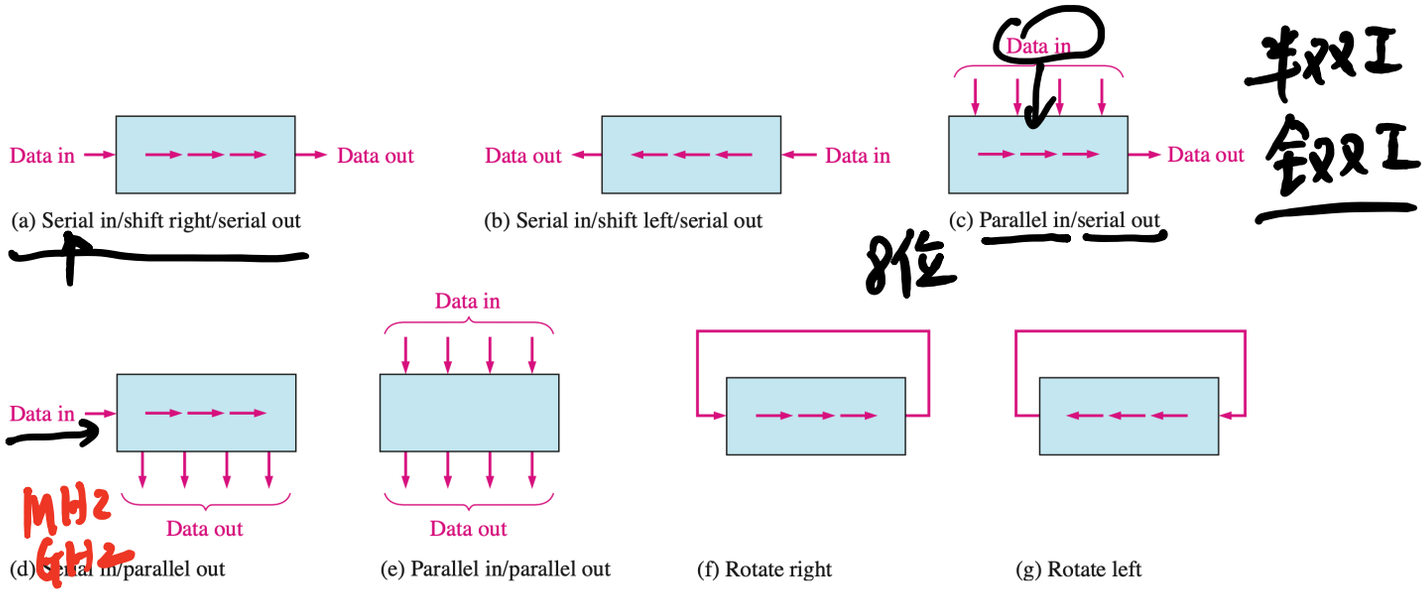


FIGURE 8–2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

Types of Shift Register Data I/Os

Serial In/Serial Out Shift Registers

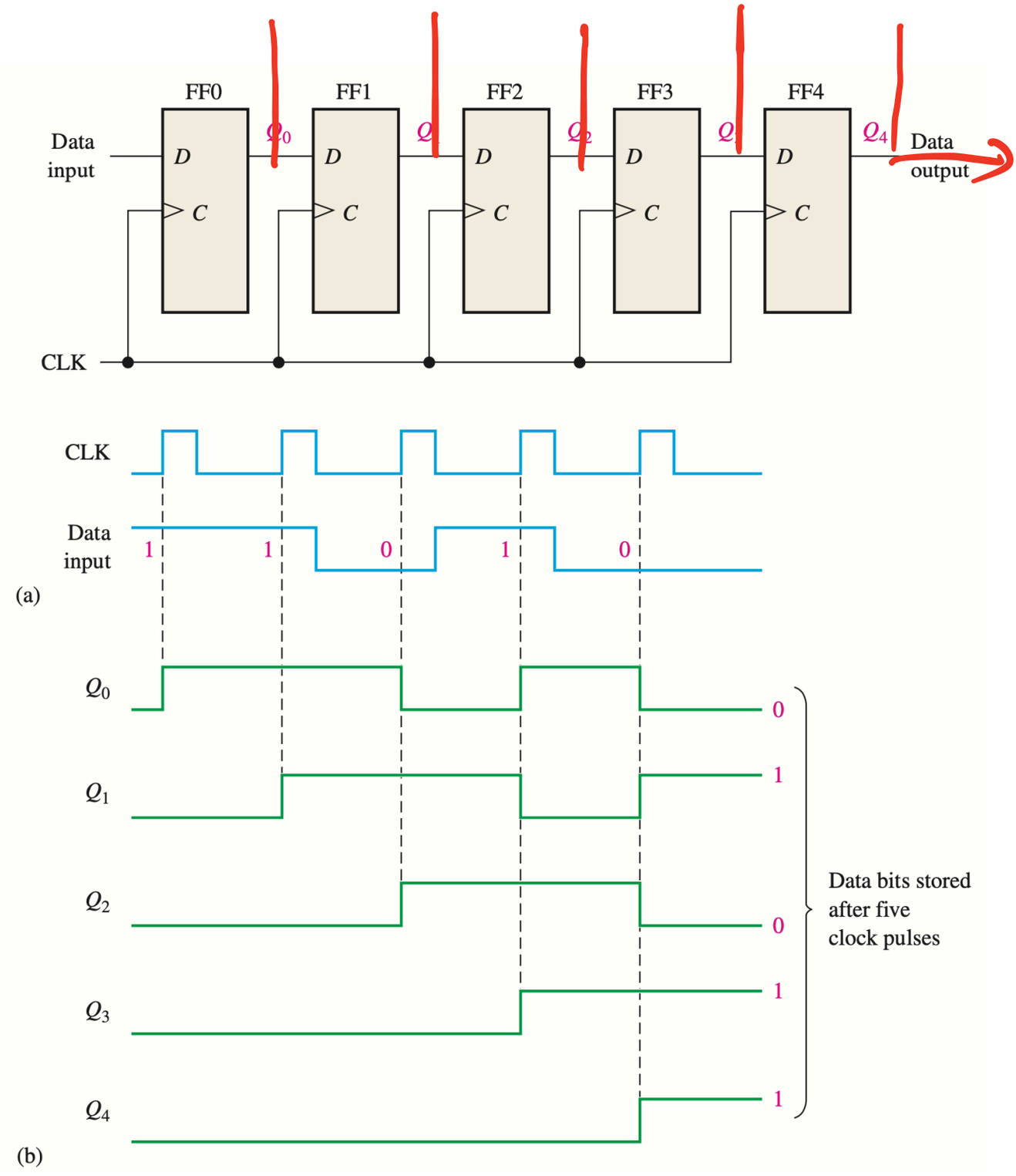


FIGURE 8–4 Open file F08-04 to verify operation. *A Multisim tutorial is available on*

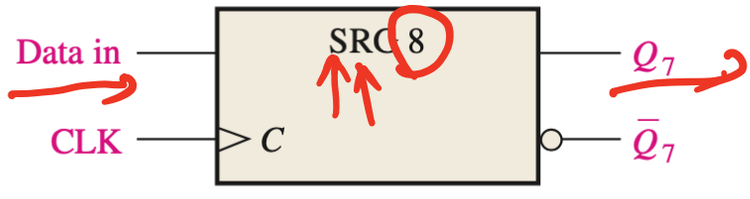


FIGURE 8–5 Logic symbol for an 8-bit serial in/serial out shift register.

Serial In/Parallel Out Shift Registers

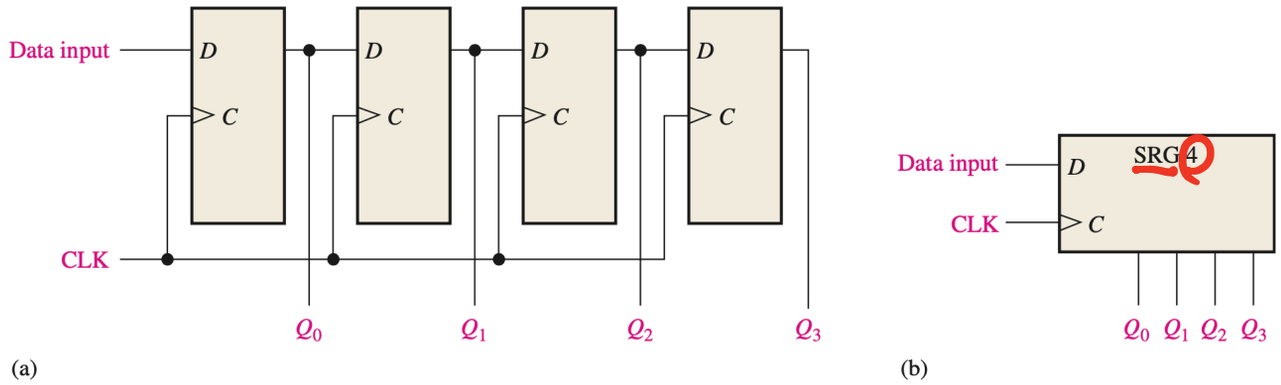


FIGURE 8–6 A serial in/parallel out shift register.

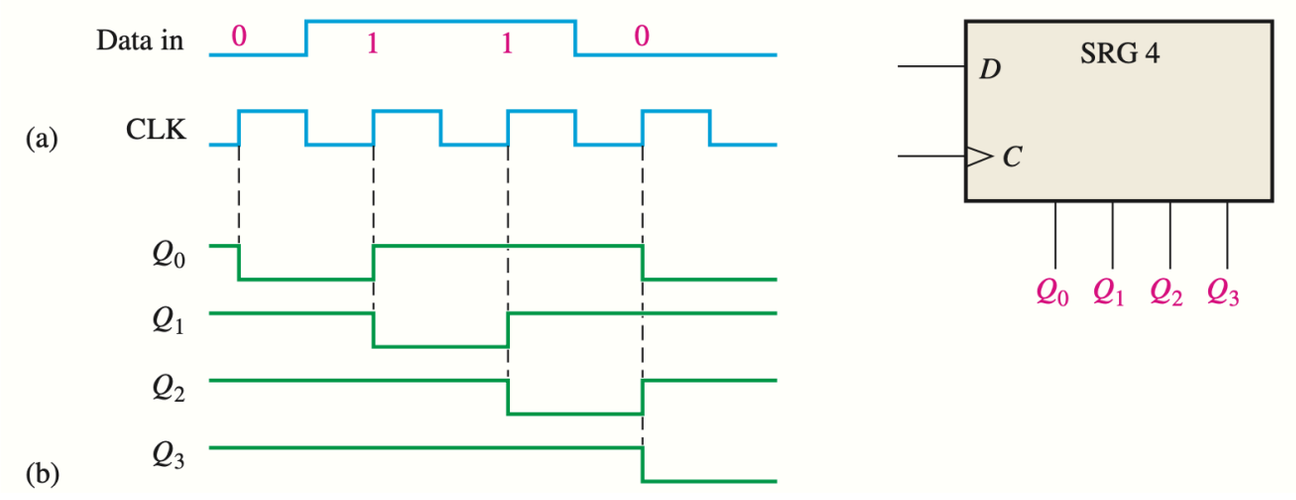
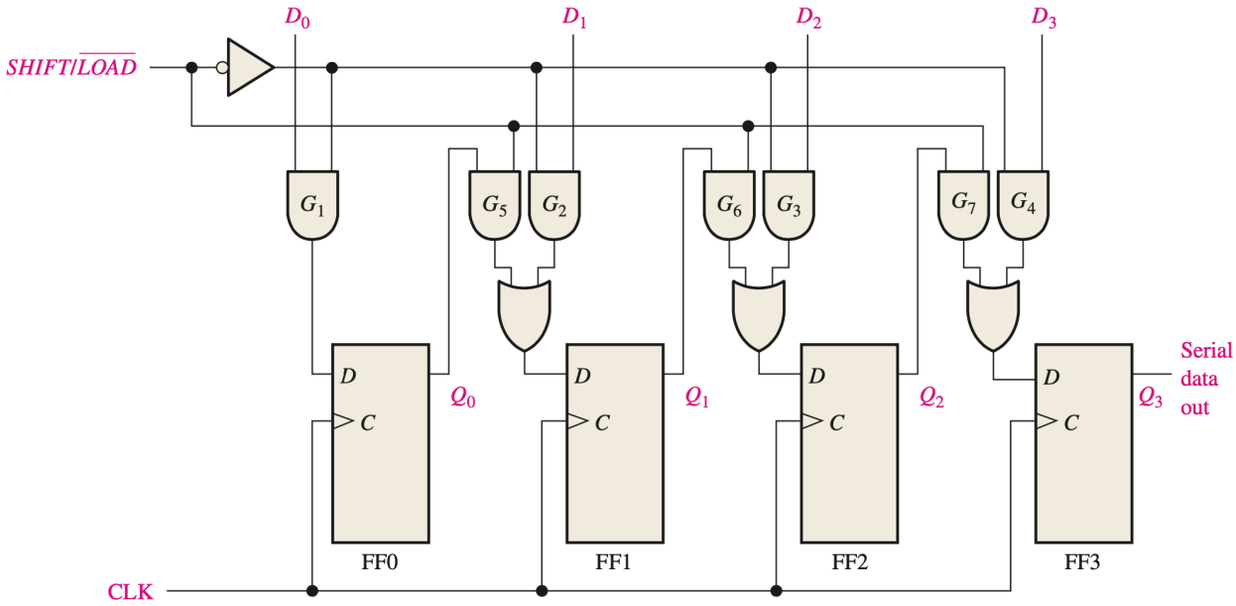
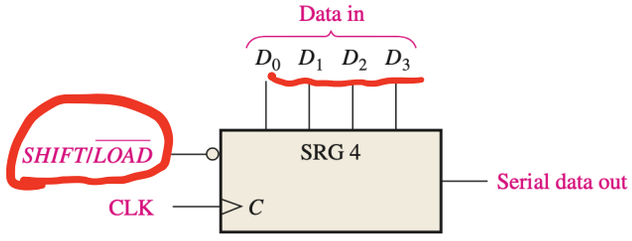


FIGURE 8–7

Parallel In/Serial Out Shift Registers



(a) Logic diagram



(b) Logic symbol

FIGURE 8–10 A 4-bit parallel in/serial out shift register. Open file F08-10 to verify operation.

MultiSim

EXAMPLE 8–3

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 8–11(a). Refer to Figure 8–10(a) for the logic diagram.

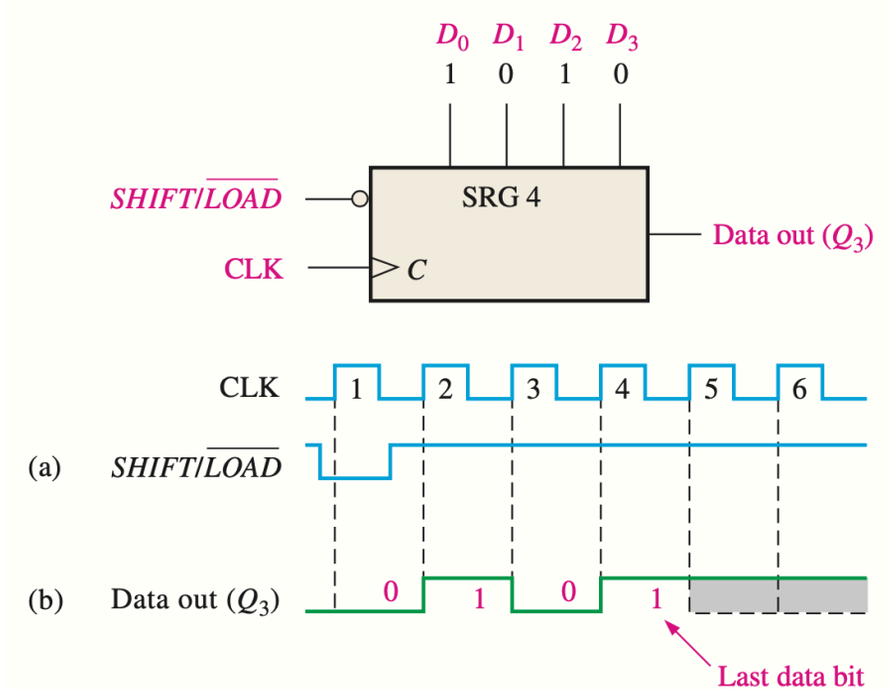
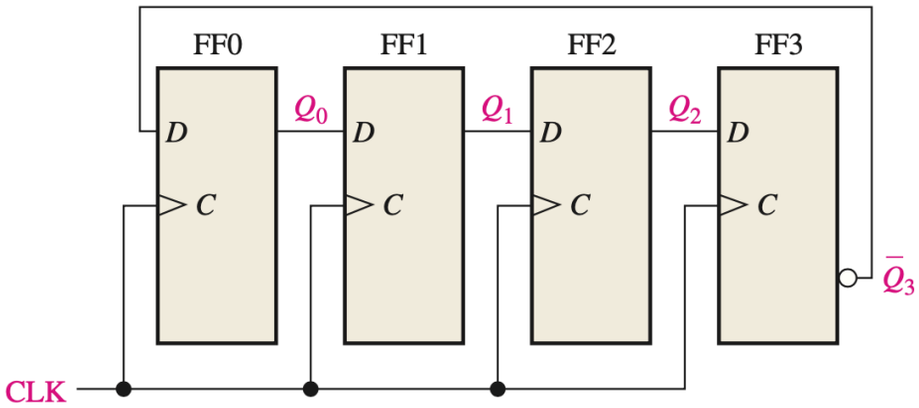


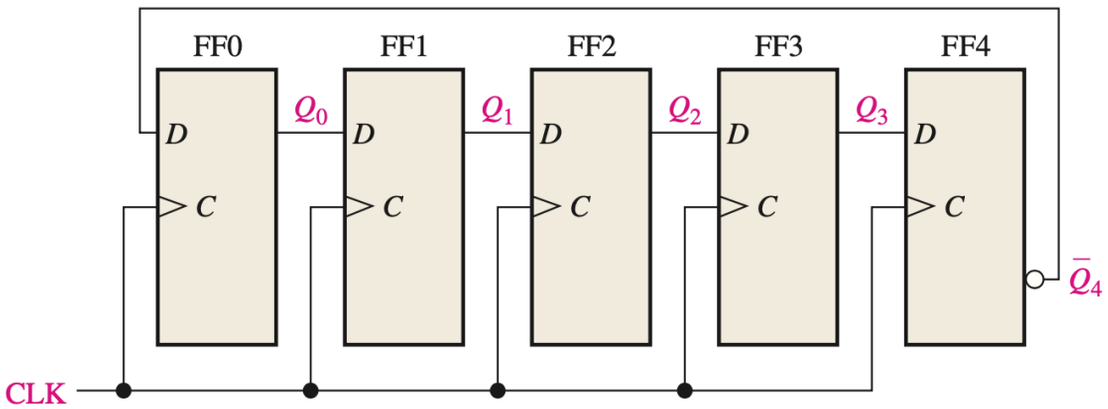
FIGURE 8–11

Shift Register Counters

The Johnson Counter

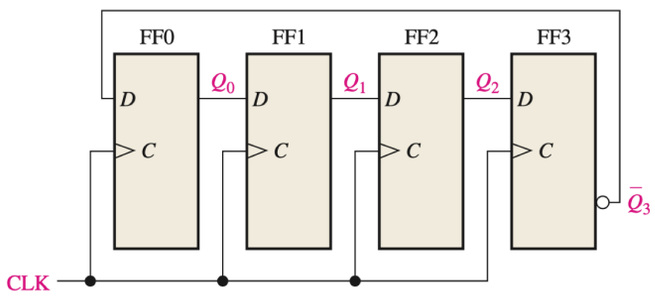


(a) Four-bit Johnson counter

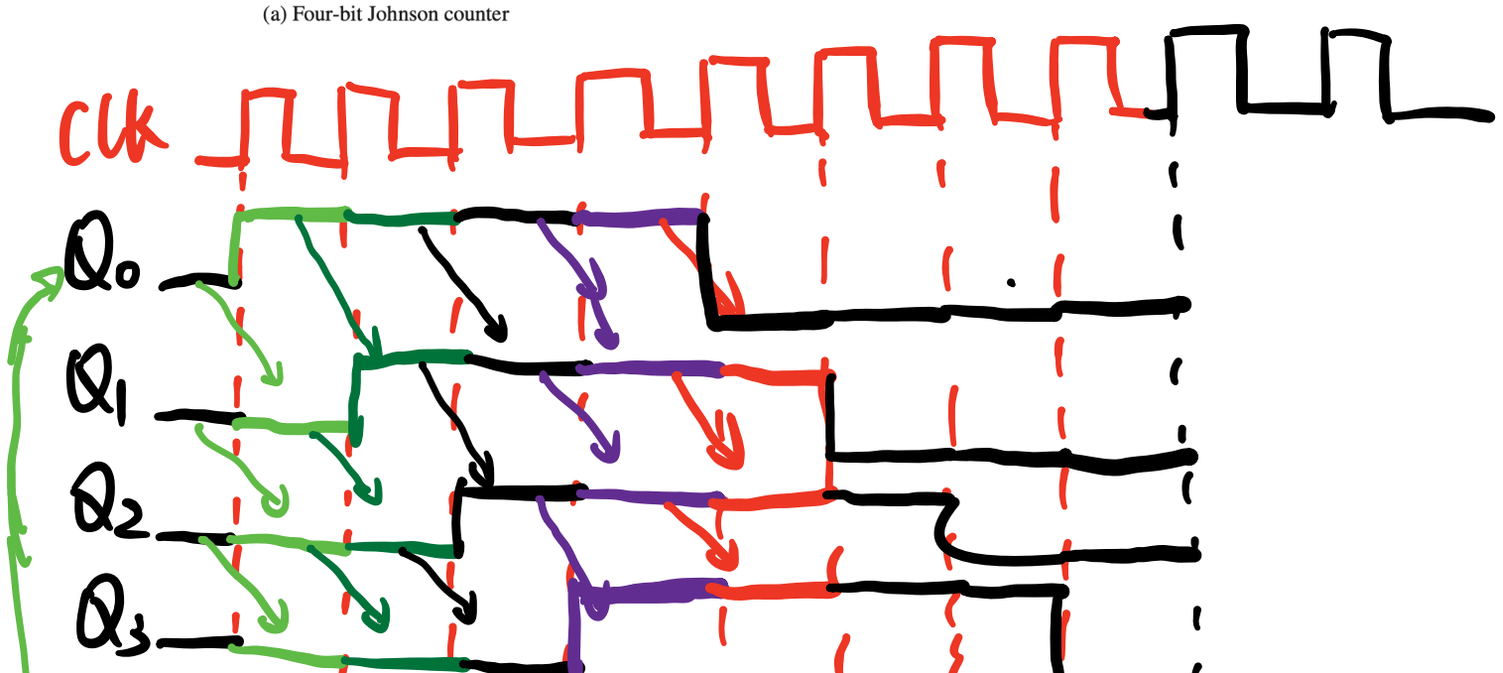


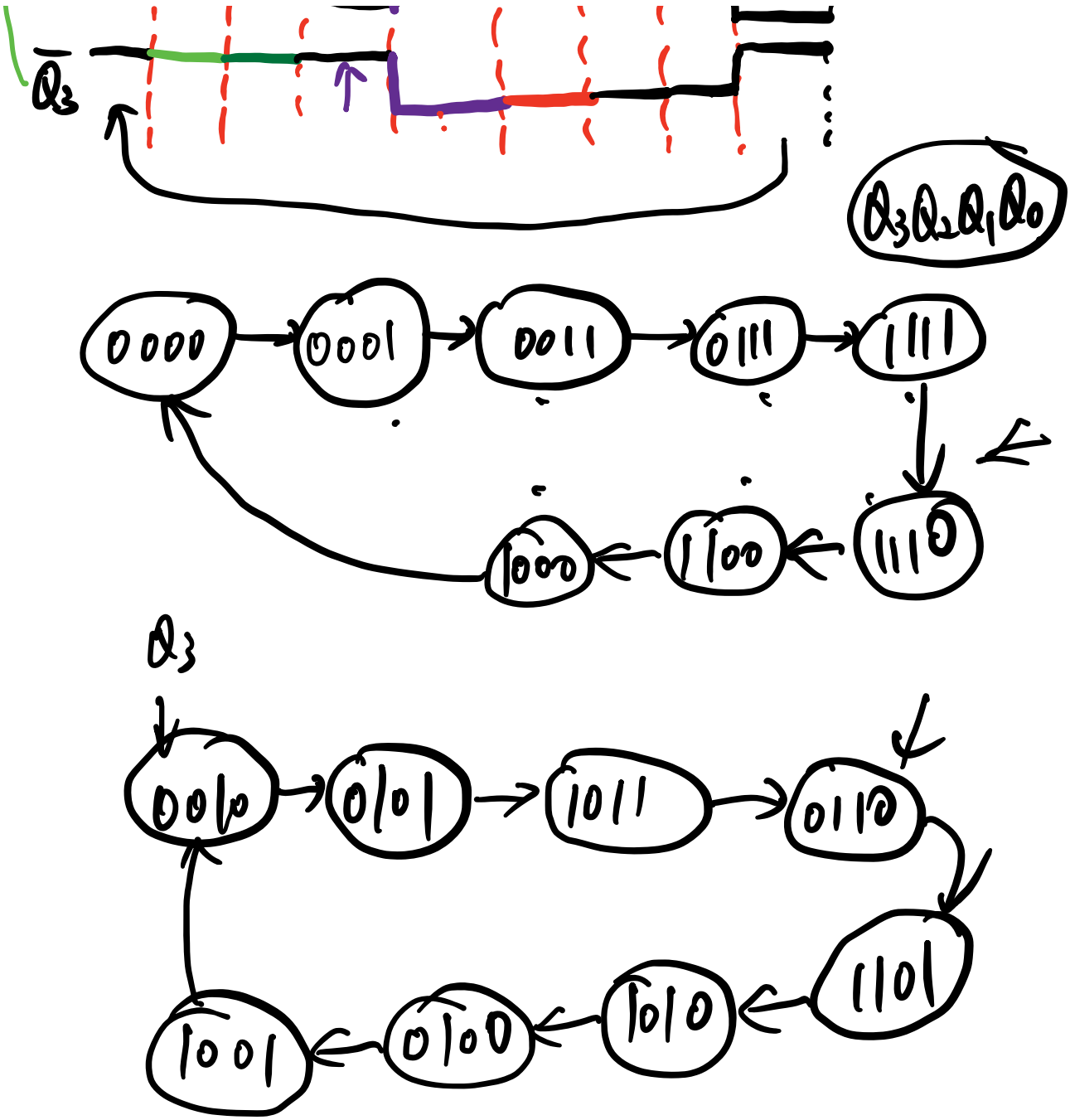
(b) Five-bit Johnson counter

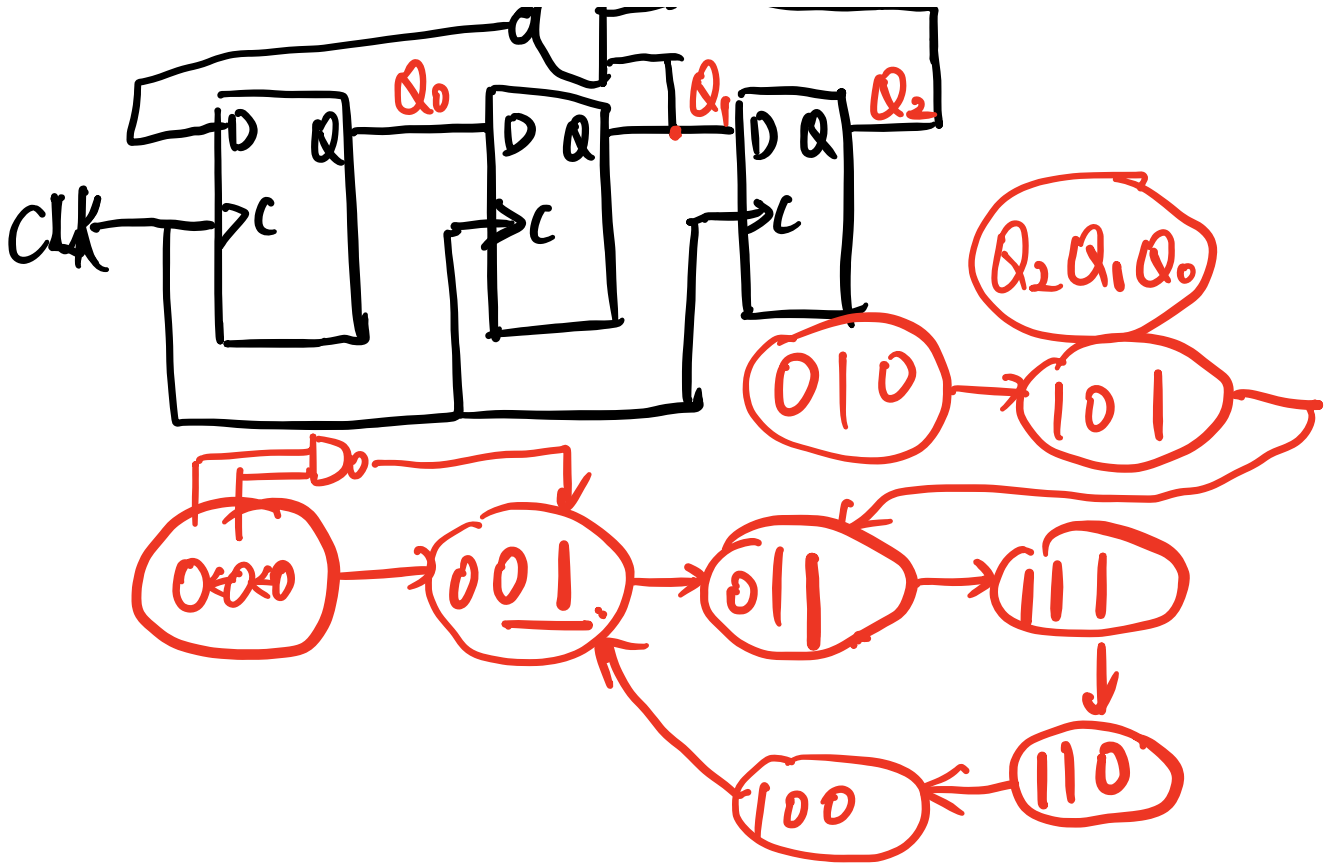
FIGURE 8–21 Four-bit and 5-bit Johnson counters.

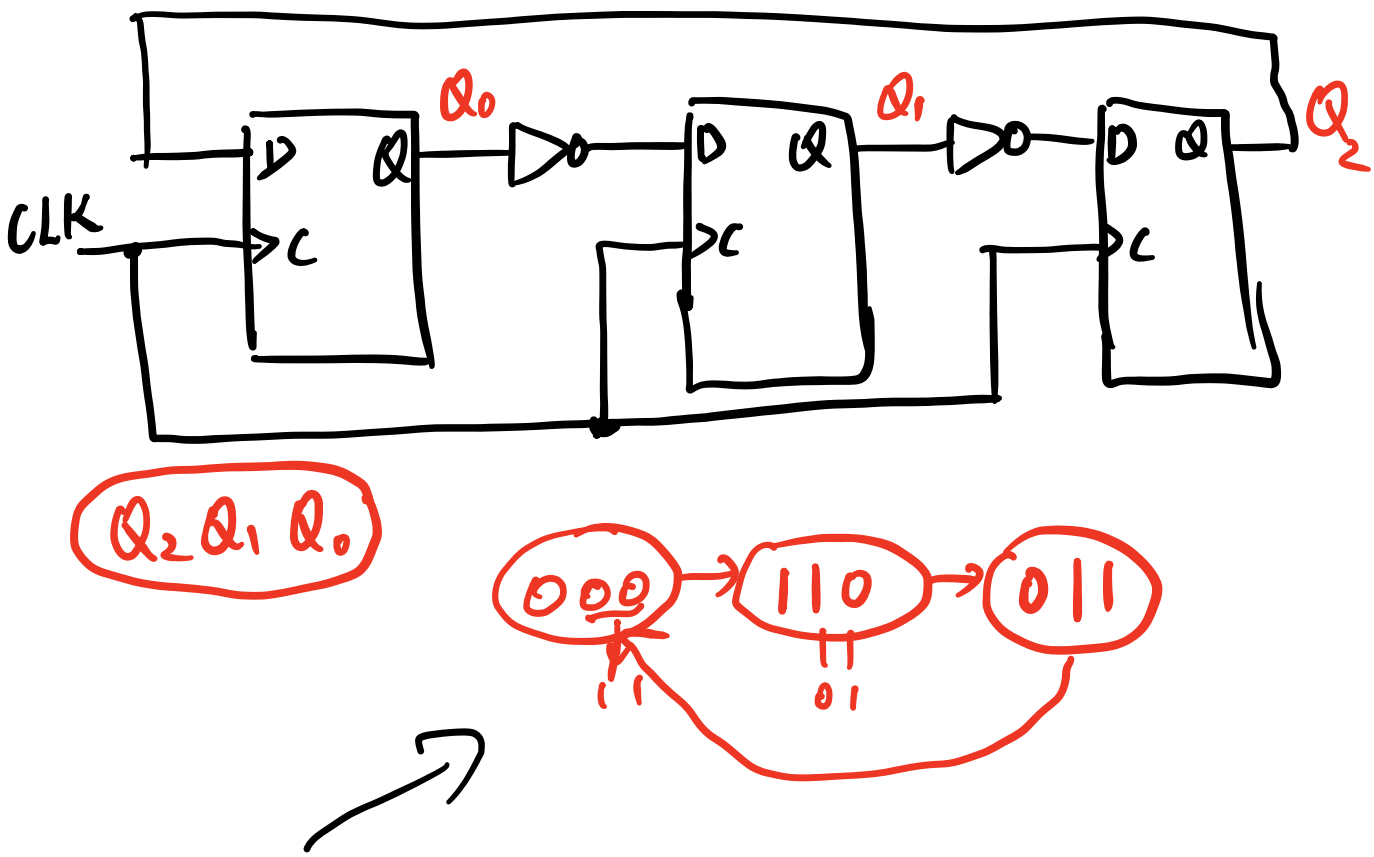


(a) Four-bit Johnson counter




$\bar{Q}_3$
$Q_3Q_2Q_1Q_0$
0000
0001
0011
0111
1111
1110
1100
1000
Q_3
0010
0101
1011
0110
1101
1010
0100
1001


Q0
Q1
Q2
D
Q
C
CLK
Q2Q1Q0
010
101
D0
000
001
011
111
110
100


Q0
Q1
Q2
D
Q
C
CLK
Q2Q1Q0
000
110
011
11
01

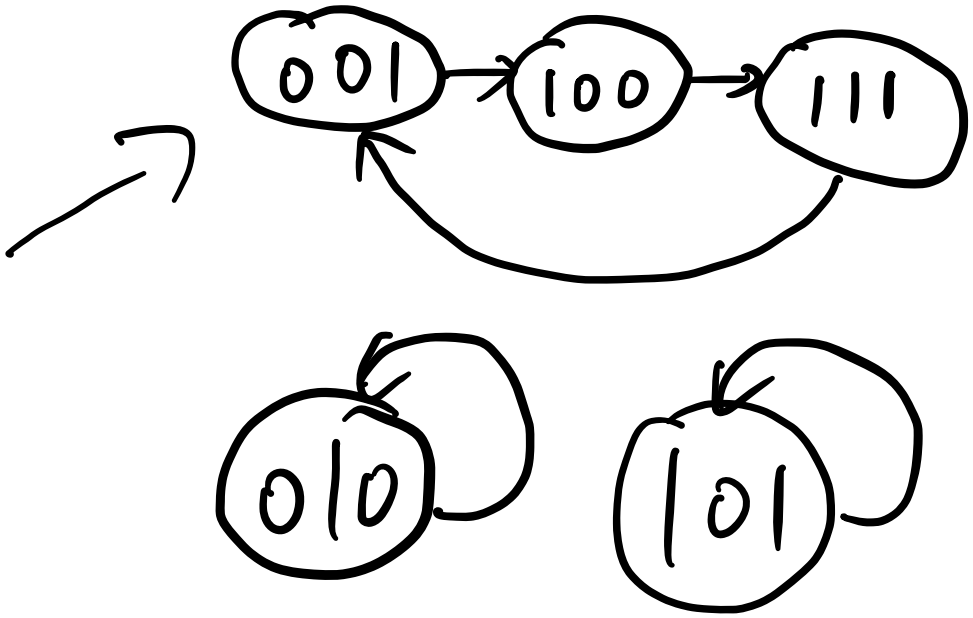

001
100
111
010
101

TABLE 8–3

Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

TABLE 8–4

Five-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

The Ring Counter

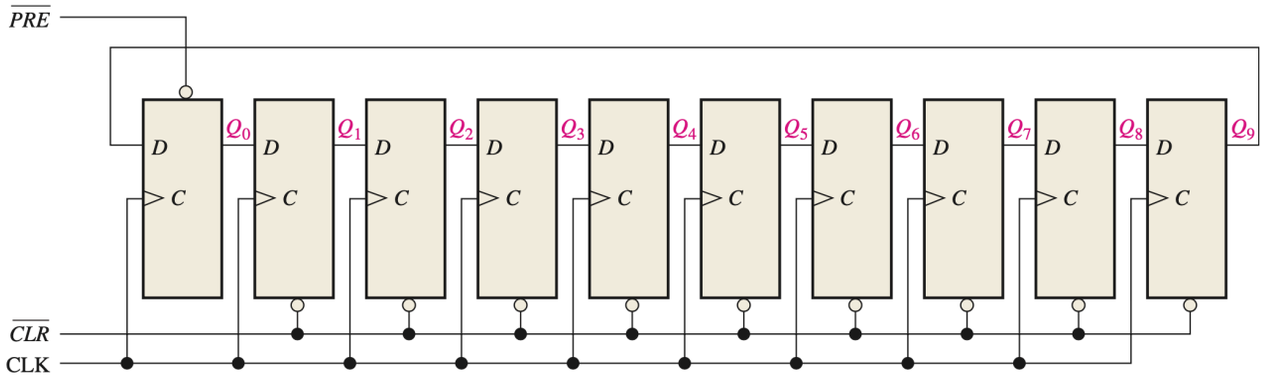


FIGURE 8–24 A 10-bit ring counter. Open file F08-24 to verify operation.

MultiSim

TABLE 8–5

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Shift Register Applications

Time Delay

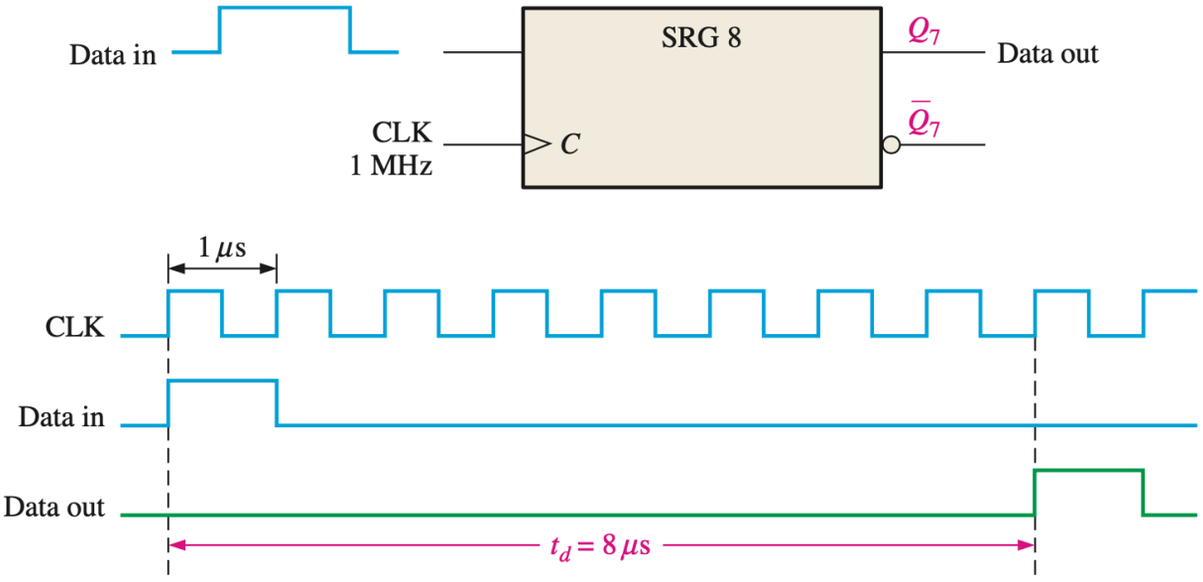


FIGURE 8–26 The shift register as a time-delay device.

Serial-to-Parallel Data Converter

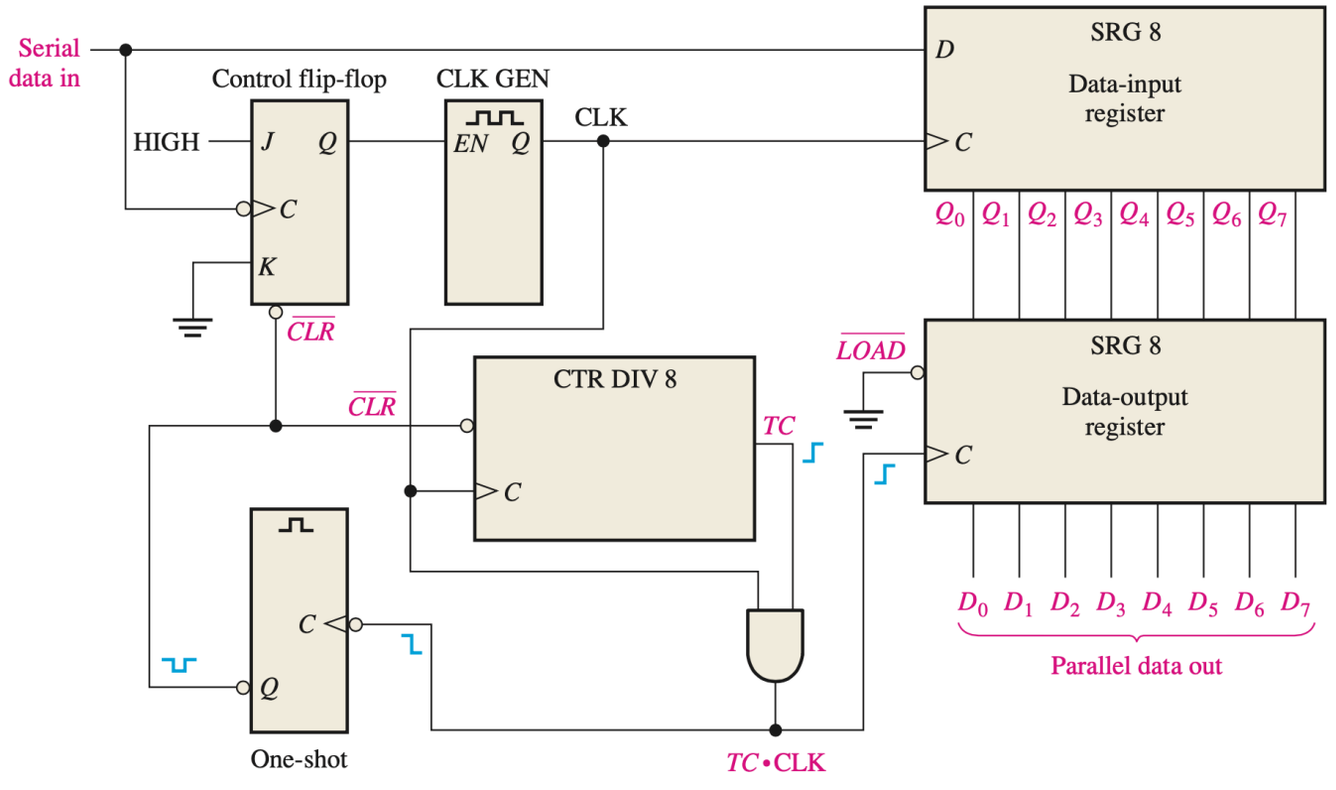


FIGURE 8–31 Simplified logic diagram of a serial-to-parallel converter.

Universal Asynchronous Receiver Transmitter (UART)

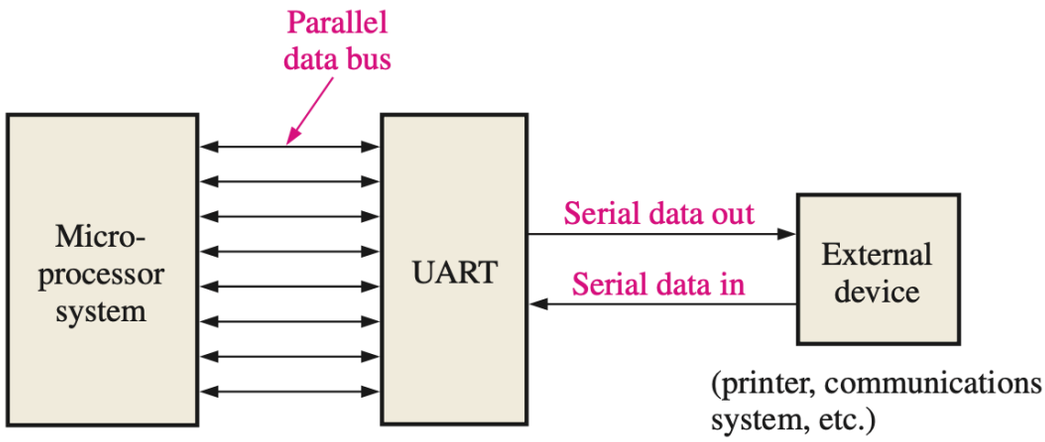


FIGURE 8–34 UART interface.

Keyboard Encoder

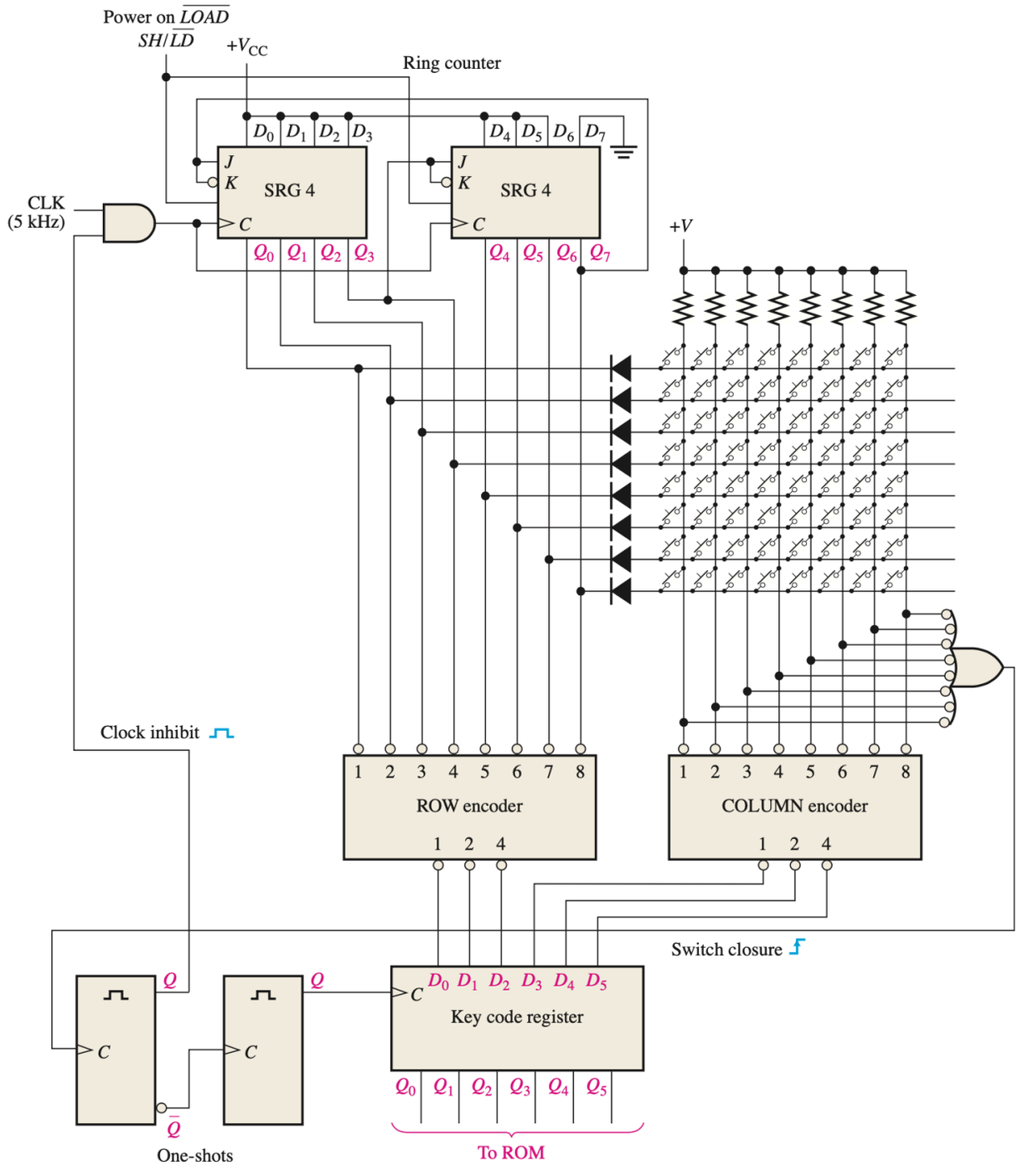


FIGURE 8–36 Simplified keyboard encoding circuit.